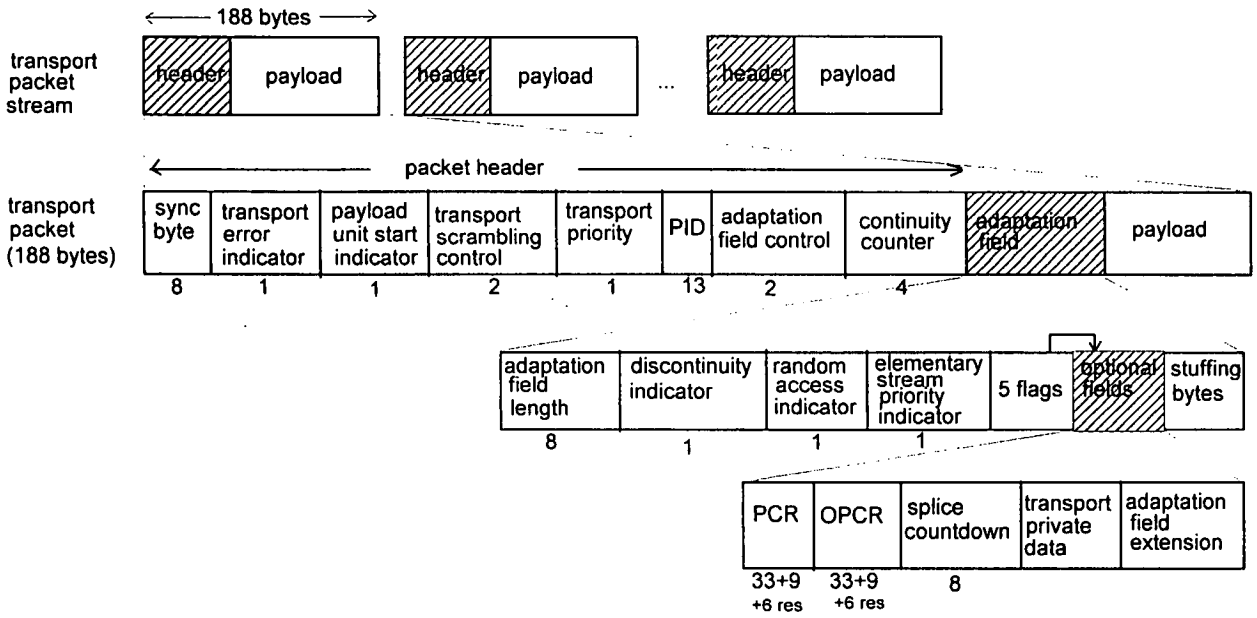
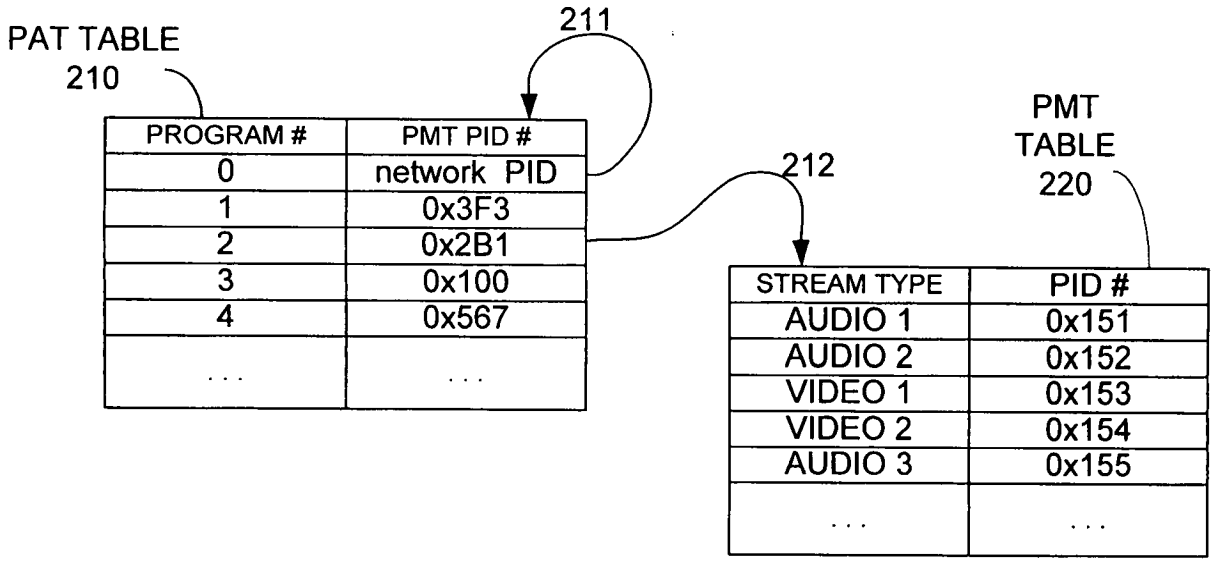


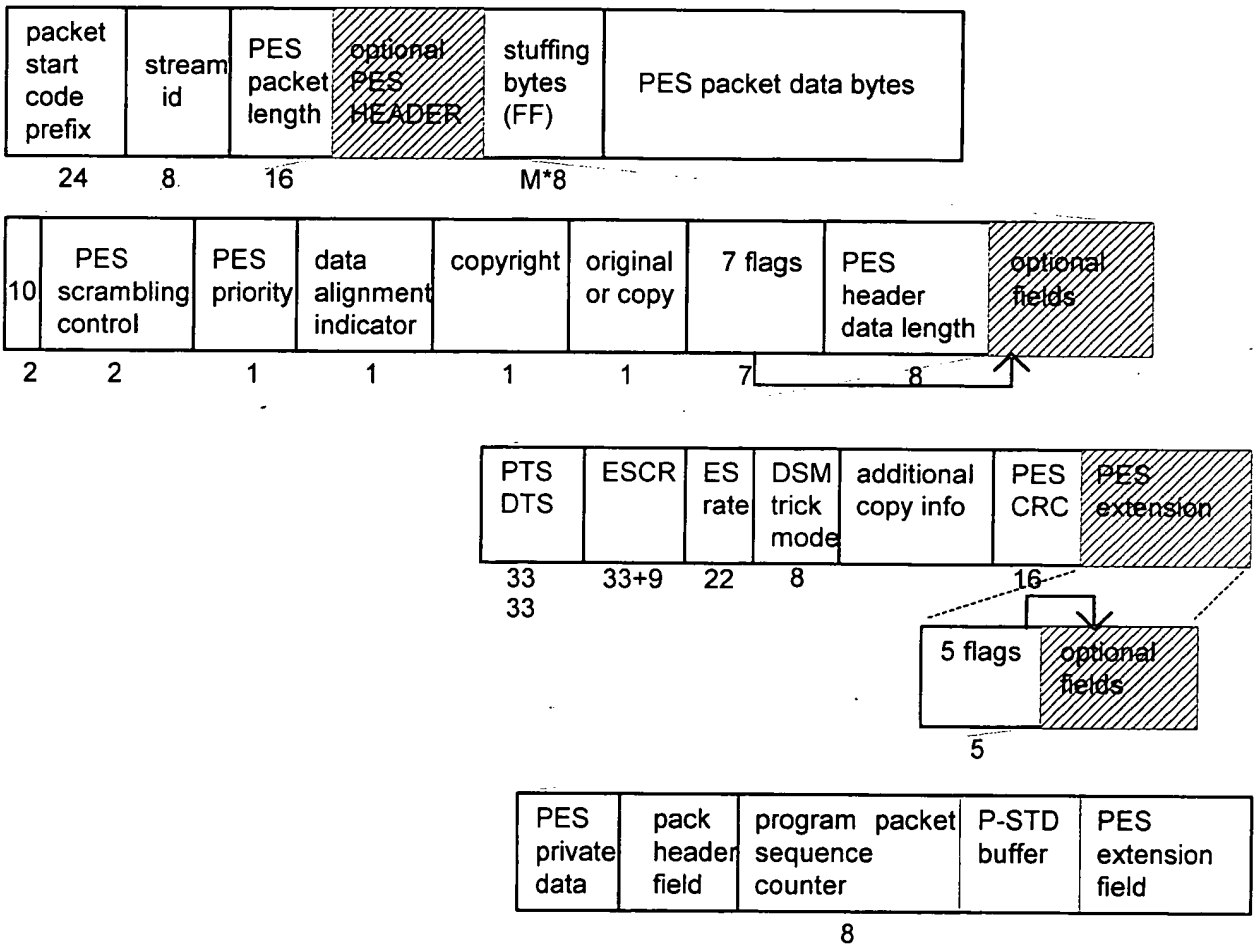
--PRIOR ART--

FIGURE 1



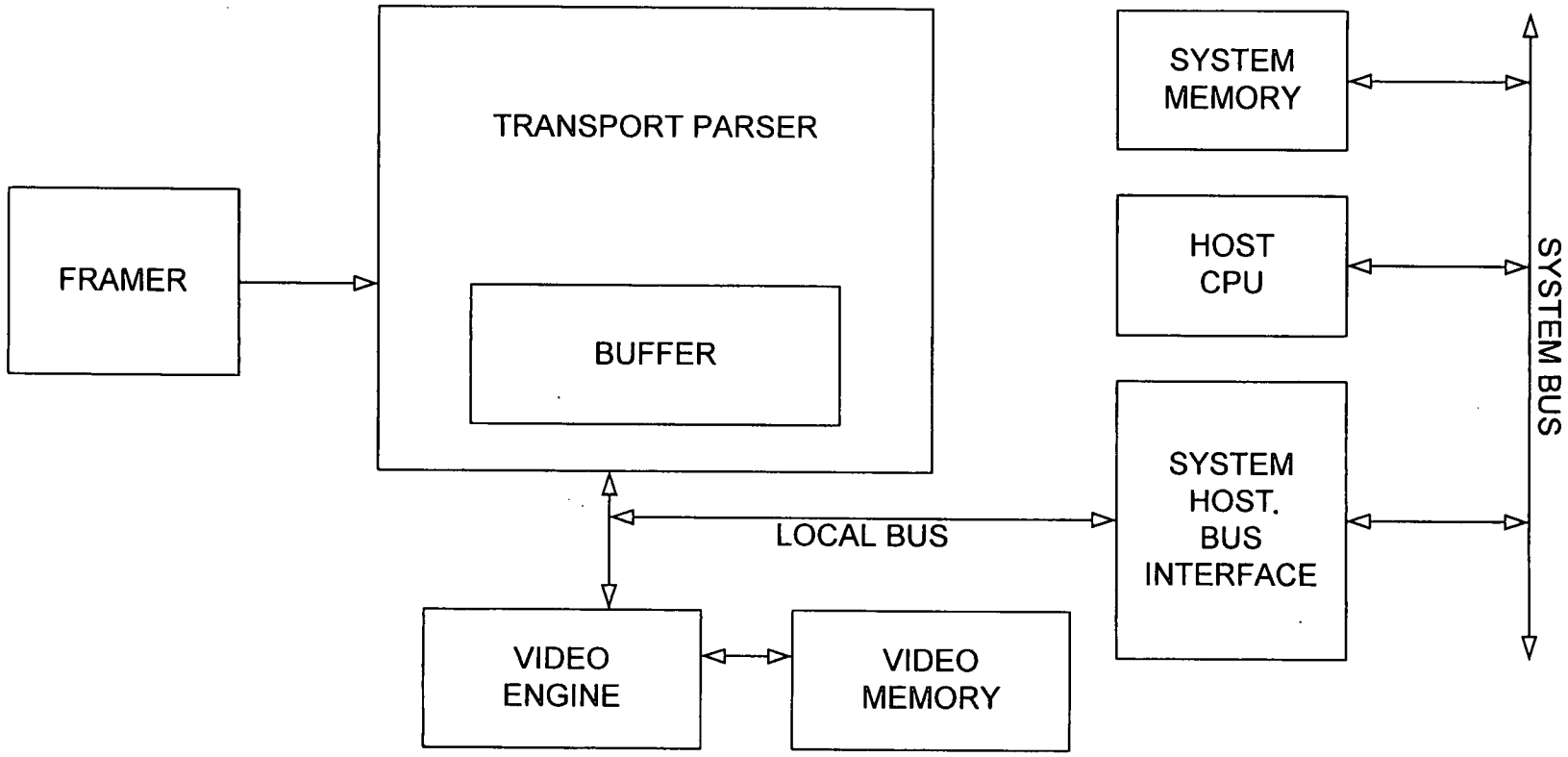
--PRIOR ART--

FIGURE 2



--PRIOR ART--

FIGURE 3



-- PRIOR ART --
FIGURE 4

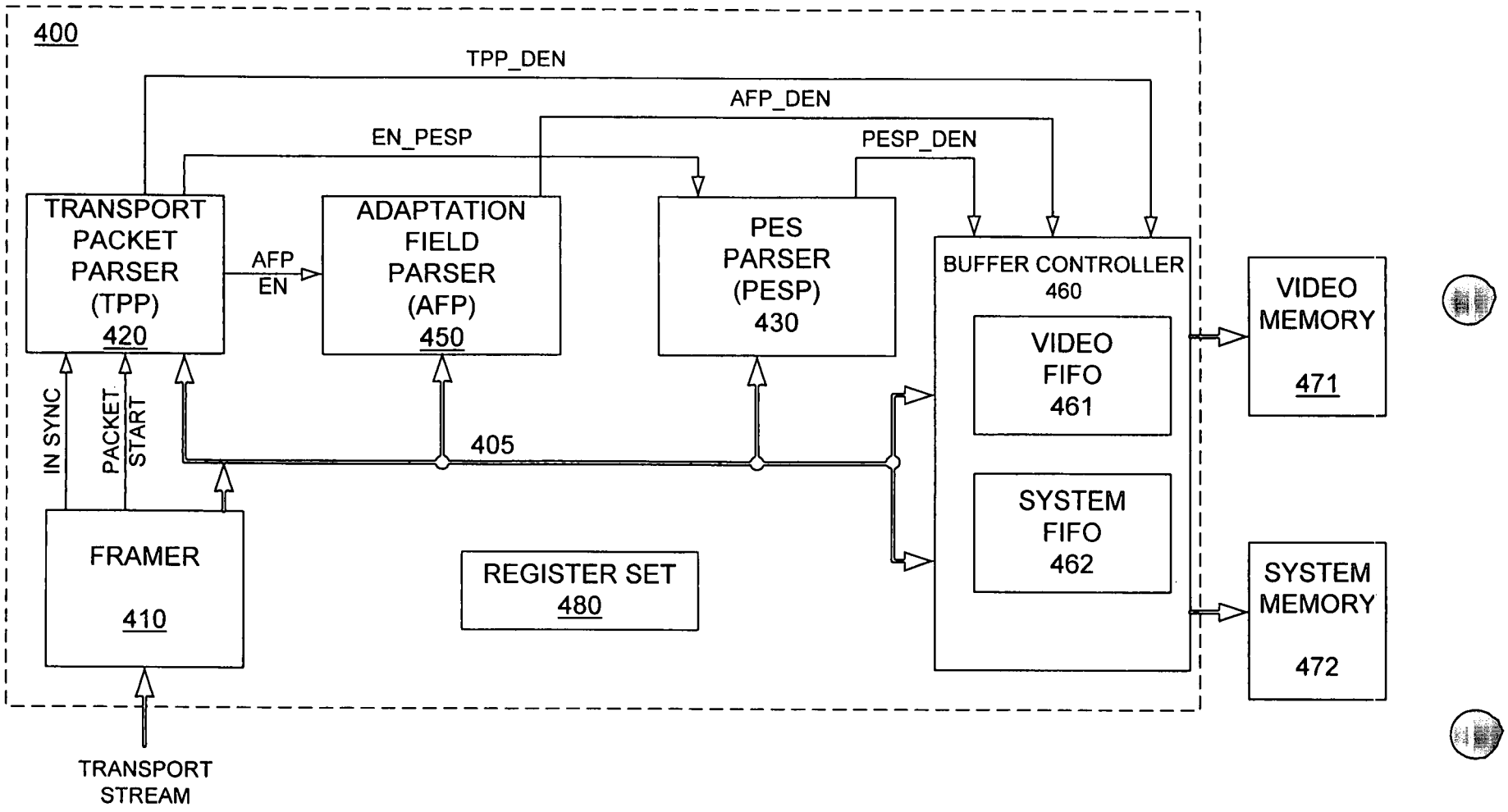

400
TPP_DEN
AFP_DEN
EN_PESP
PESP_DEN
TRANSPORT PACKET PARSER (TPP) 420
AFP EN
ADAPTATION FIELD PARSER (AFP) 450
PES PARSER (PESP) 430
BUFFER CONTROLLER 460
VIDEO FIFO 461
SYSTEM FIFO 462
VIDEO MEMORY 471
SYSTEM MEMORY 472
IN SYNC
PACKET START
405
FRAMER 410
REGISTER SET 480
TRANSPORT STREAM

FIGURE 5

480

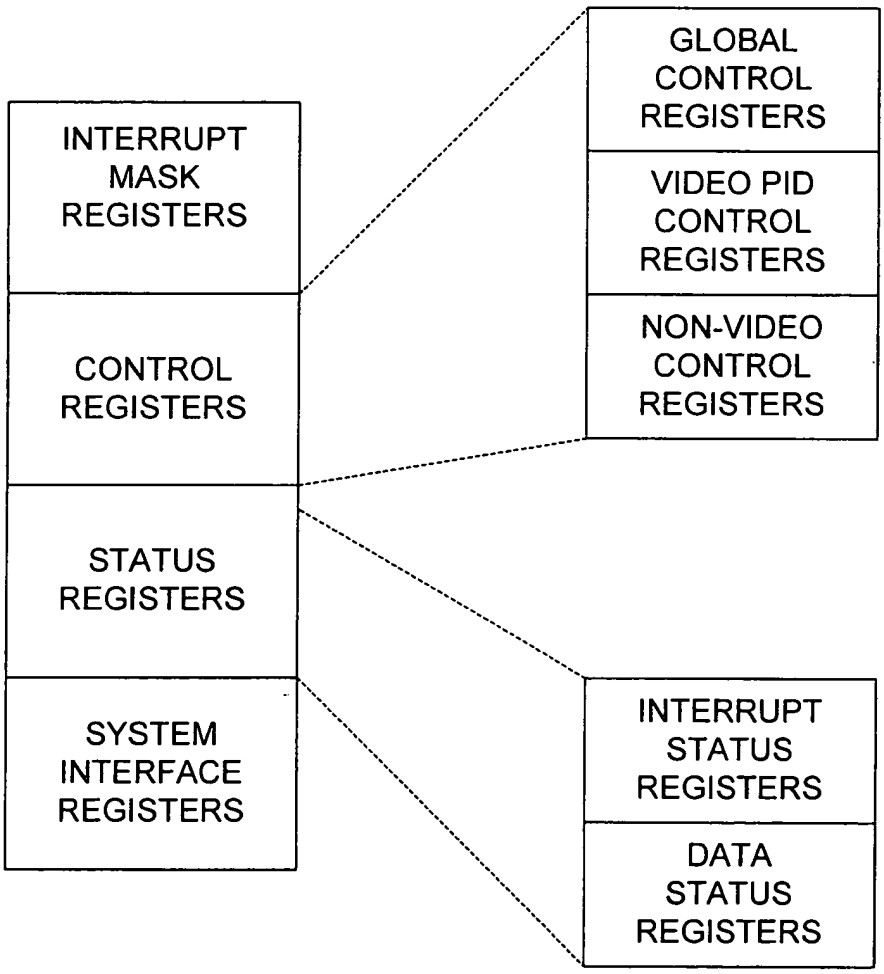

INTERRUPT MASK REGISTERS
CONTROL REGISTERS
STATUS REGISTERS
SYSTEM INTERFACE REGISTERS
GLOBAL CONTROL REGISTERS
VIDEO PID CONTROL REGISTERS
NON-VIDEO CONTROL REGISTERS
INTERRUPT STATUS REGISTERS
DATA STATUS REGISTERS

FIGURE 6

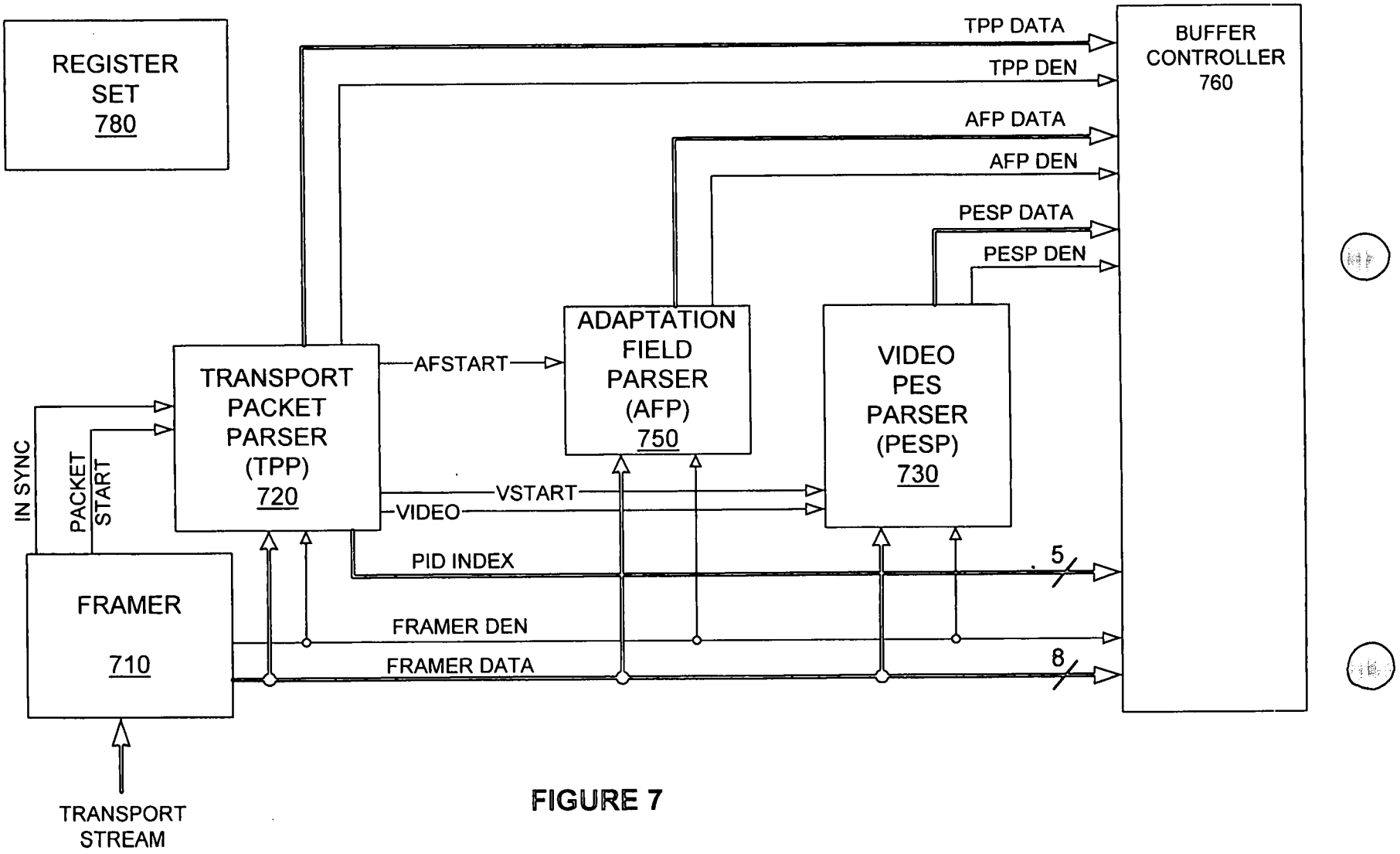


FIGURE 7

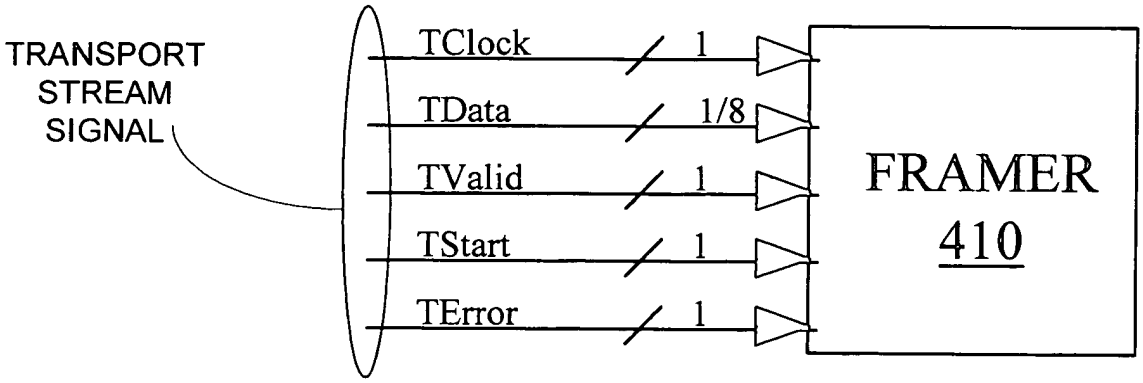


FIGURE 8

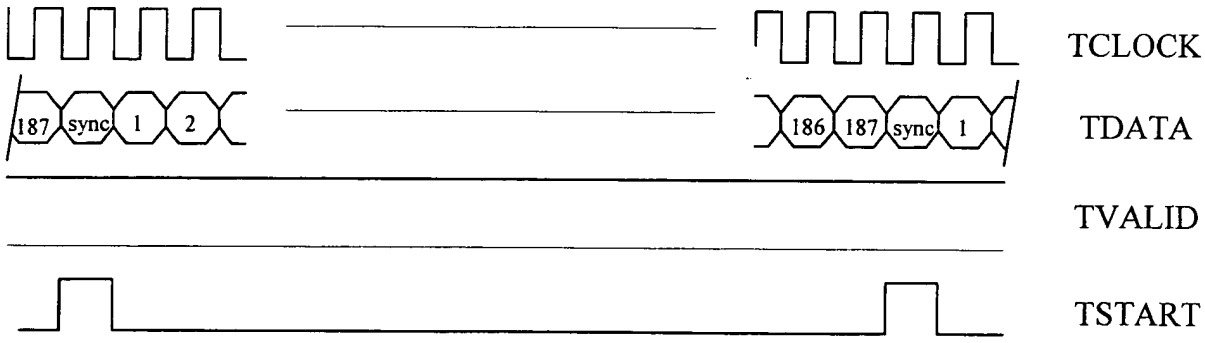


FIGURE 9

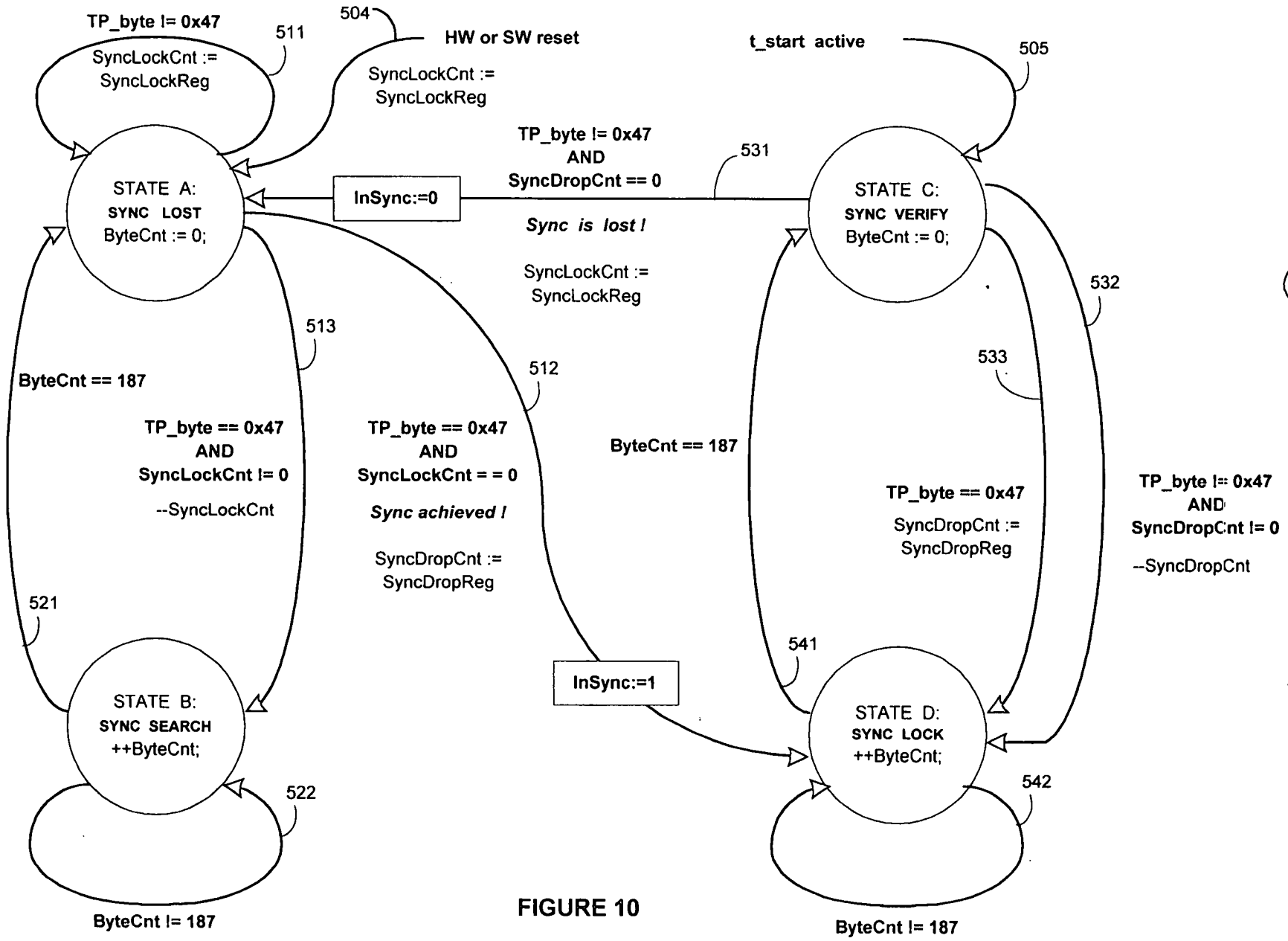

TP_byte != 0x47
SyncLockCnt :=
SyncLockReg
511
504
HW or SW reset
SyncLockCnt :=
SyncLockReg
t_start active
505
TP_byte != 0x47
AND
SyncDropCnt == 0
531
STATE A:
SYNC LOST
ByteCnt := 0;
InSync:=0
Sync is lost !
SyncLockCnt :=
SyncLockReg
STATE C:
SYNC VERIFY
ByteCnt := 0;
532
513
512
533
ByteCnt == 187
TP_byte == 0x47
AND
SyncLockCnt != 0
--SyncLockCnt
TP_byte == 0x47
AND
SyncLockCnt = = 0
Sync achieved !
SyncDropCnt :=
SyncDropReg
ByteCnt == 187
TP_byte == 0x47
SyncDropCnt :=
SyncDropReg
TP_byte != 0x47
AND
SyncDropCnt != 0
--SyncDropCnt
521
541
InSync:=1
STATE B:
SYNC SEARCH
++ByteCnt;
STATE D:
SYNC LOCK
++ByteCnt;
522
542
ByteCnt != 187
ByteCnt != 187

FIGURE 10

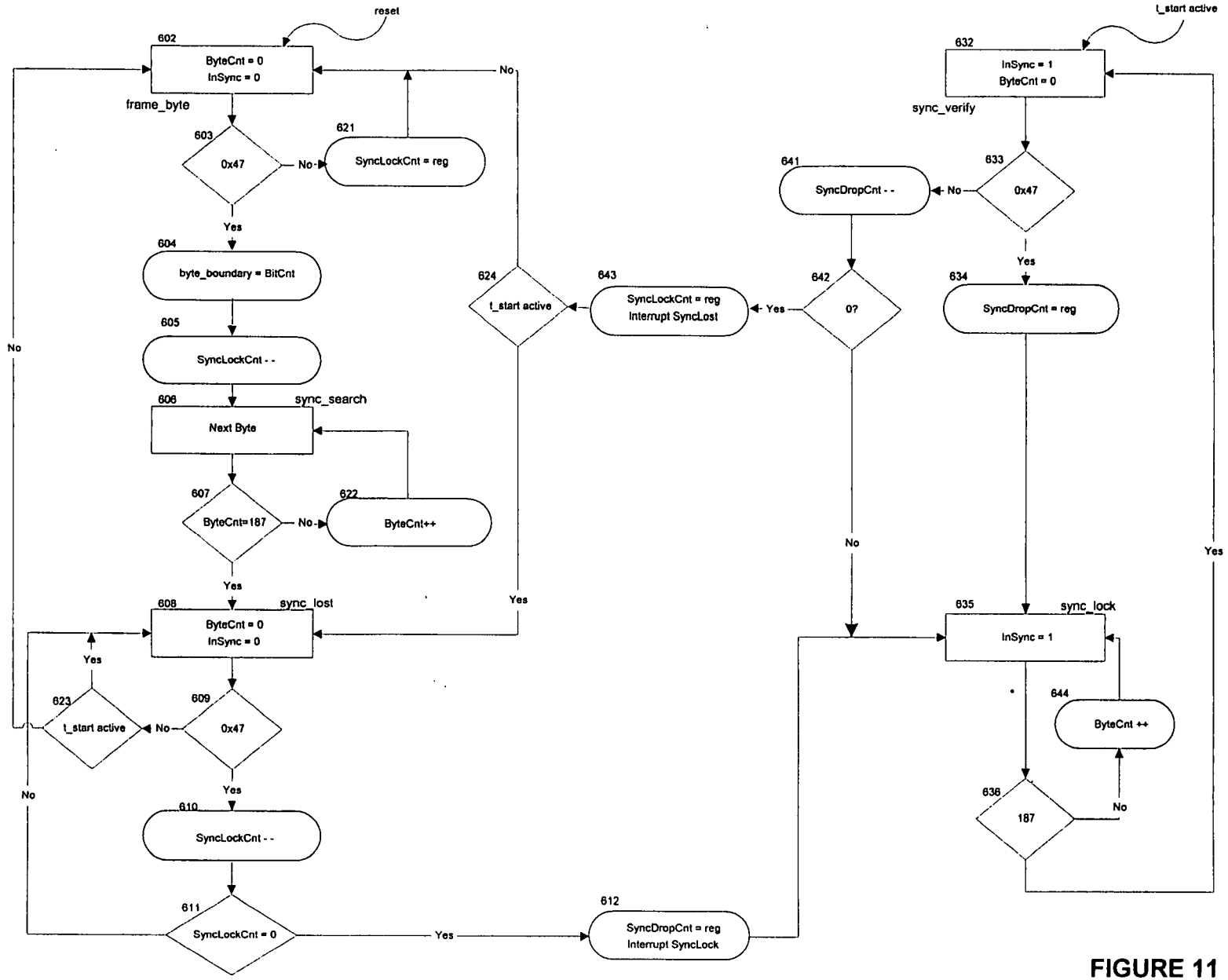

reset
602
ByteCnt = 0
InSync = 0
frame_byte
603
0x47
No
621
SyncLockCnt = reg
Yes
604
byte_boundary = BitCnt
605
SyncLockCnt - -
606
sync_search
Next Byte
607
ByteCnt=187
No
622
ByteCnt++
Yes
608
sync_lost
ByteCnt = 0
InSync = 0
623
t_start active
No
609
0x47
Yes
610
SyncLockCnt - -
611
SyncLockCnt = 0
Yes
612
SyncDropCnt = reg
Interrupt SyncLock
No
624
t_start active
No
643
SyncLockCnt = reg
Interrupt SyncLost
Yes
642
0?
No
641
SyncDropCnt - -
No
633
0x47
Yes
634
SyncDropCnt = reg
t_start active
632
InSync = 1
ByteCnt = 0
sync_verify
Yes
635
sync_lock
InSync = 1
644
ByteCnt ++
636
187
No

FIGURE 11

Transport Demultiplexer Global Status Register				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
FramerSyncLock	0	[1] 0	R/W	This bit is set to '1' after the frame synchronization has been acquired. **WR_ACC_CLEAR.**
FramerSyncDrop	1	[1] 0	R/W	This bit is set to '1' after the frame synchronization has been lost. **WR_ACC_CLEAR.**
CurrentFramerState	20-22	[3] '000'	R	This 3 bit field codes the current state of the framer: '000' – Capturing a byte '001' – Out of TP frame synchronization '010' – Searching for synchronization '011' – Checking for synchronization '100' – In the TP frame synchronization NOTE: Only a framer state machine updates this field. Write access does not modify it.
UnusedField	29-31	[3] '000'	R/W	Unused and reserved field.

FIGURE 12

Transport Demultiplexer Interrupt Mask Register				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
EventInterruptMask	0-18	[19] 0	R/W	If set to '1' enables local sources of interrupts. Bit 0 – FramerSyncLock Bit 1 – FramerSyncDrop Bits 2 – 19 Other Functionality
EnableGlobalDemuxInterrupt	20	[1] 0	R/W	If set to '1' enables globally TD core interrupts.
UnusedField	21-31	[11] 0	R/W	Unused and reserved field. Always set to 0.

FIGURE 13

Transport Demultiplexer Global Control Register					
Field Name	**Bits**	**Len**	**Default**	**Type**	**Description**
FramerSyncLockLength	0-4	[5]	00101	R/W	Five bits field to select a number of consecutive transport packets after MPEG-2 frame (bit-stream) synchronization is declared.
FramerSyncDropLength	5-7	[3]	011	R/W	Three bits field to select a number of consecutive transport packets after a loss of MPEG-2 frame synchronization is declared.
FramerBitPolarity	8	[1]	0	R/W	'0' selects msb first (default mode), '1' select lsb first
FramerClockPolarity	9	[1]	0	R/W	If set to '0' framer will latch on falling edge (default) If set to '1' framer will latch on rising edge.
FramerMode:	10-11	[2]	'00'	R/W	Defines a combination of external control signals: '00' – Framer uses T_start only. '01' – Framer uses T_valid only. '10' – Framer uses T_start and T_valid. '11' – Framer uses T_clock and T_data only.
Other Functionality Bits	12-15	[4]			Other functionality (not relevant to Framer)
T_ValidPolarity	16	[1]	1	R/W	'1' selects active high [5V] for t_valid external signal
T_StartPolarity	17	[1]	1	R/W	'1' selects active high [5V] for t_start external signal
T_ErrorPolarity	18	[1]	1	R/W	'1' selects active high [5V] for t_error external signal
Other Functionality Bits	19-28	[10]			Other functionality (not relevant to Framer)
UnusedField	29 -31	[3]	0	R/W	Unused and reserved field. Always set to 0.

FIGURE 14

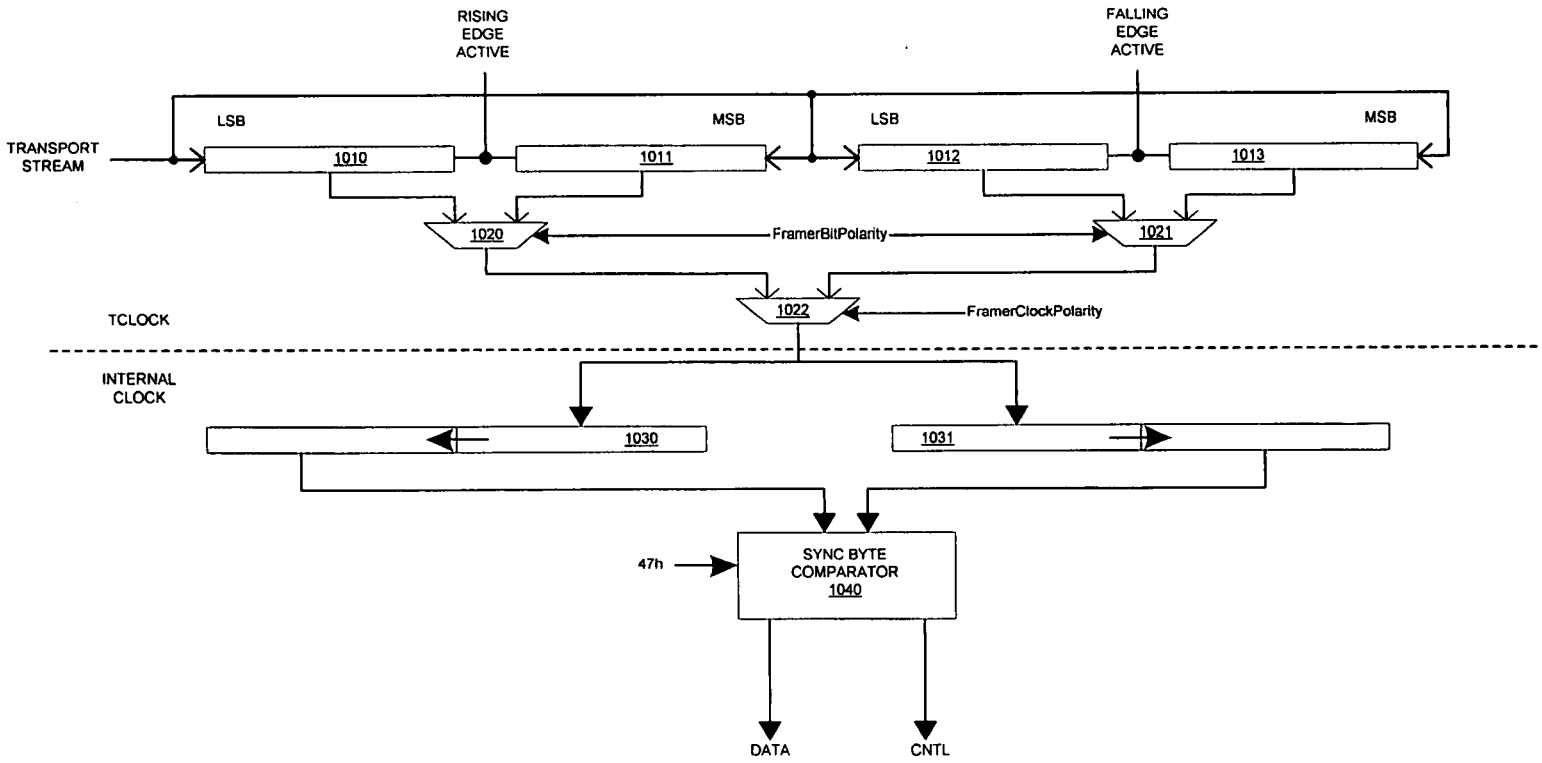


FIGURE 15

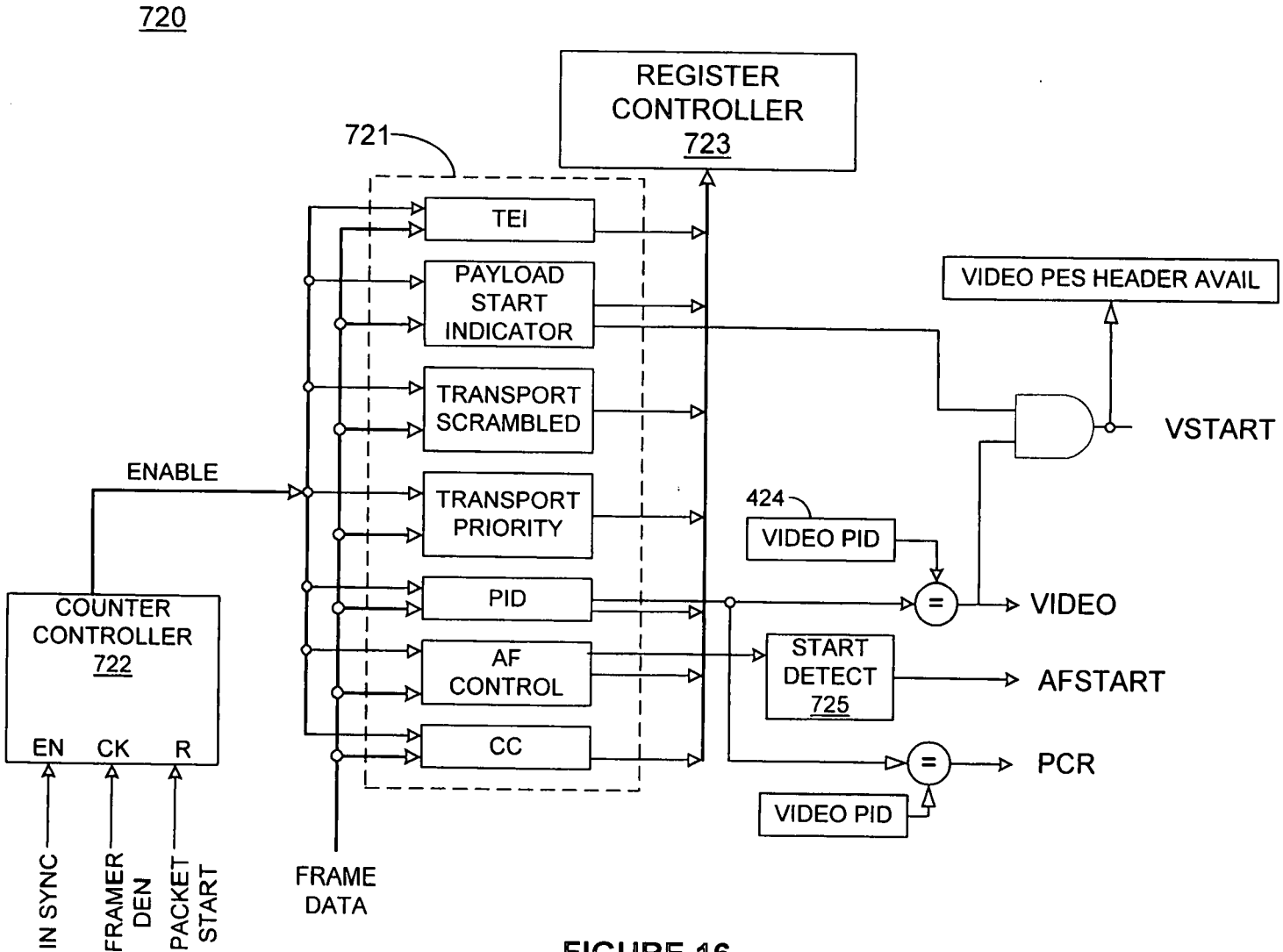

720
REGISTER CONTROLLER 723
721
TEI
PAYLOAD START INDICATOR
TRANSPORT SCRAMBLED
TRANSPORT PRIORITY
PID
AF CONTROL
CC
VIDEO PES HEADER AVAIL
VSTART
ENABLE
424
VIDEO PID
=
VIDEO
START DETECT 725
AFSTART
=
PCR
VIDEO PID
COUNTER CONTROLLER 722
EN
CK
R
IN SYNC
FRAMER DEN
PACKET START
FRAME DATA

FIGURE 16

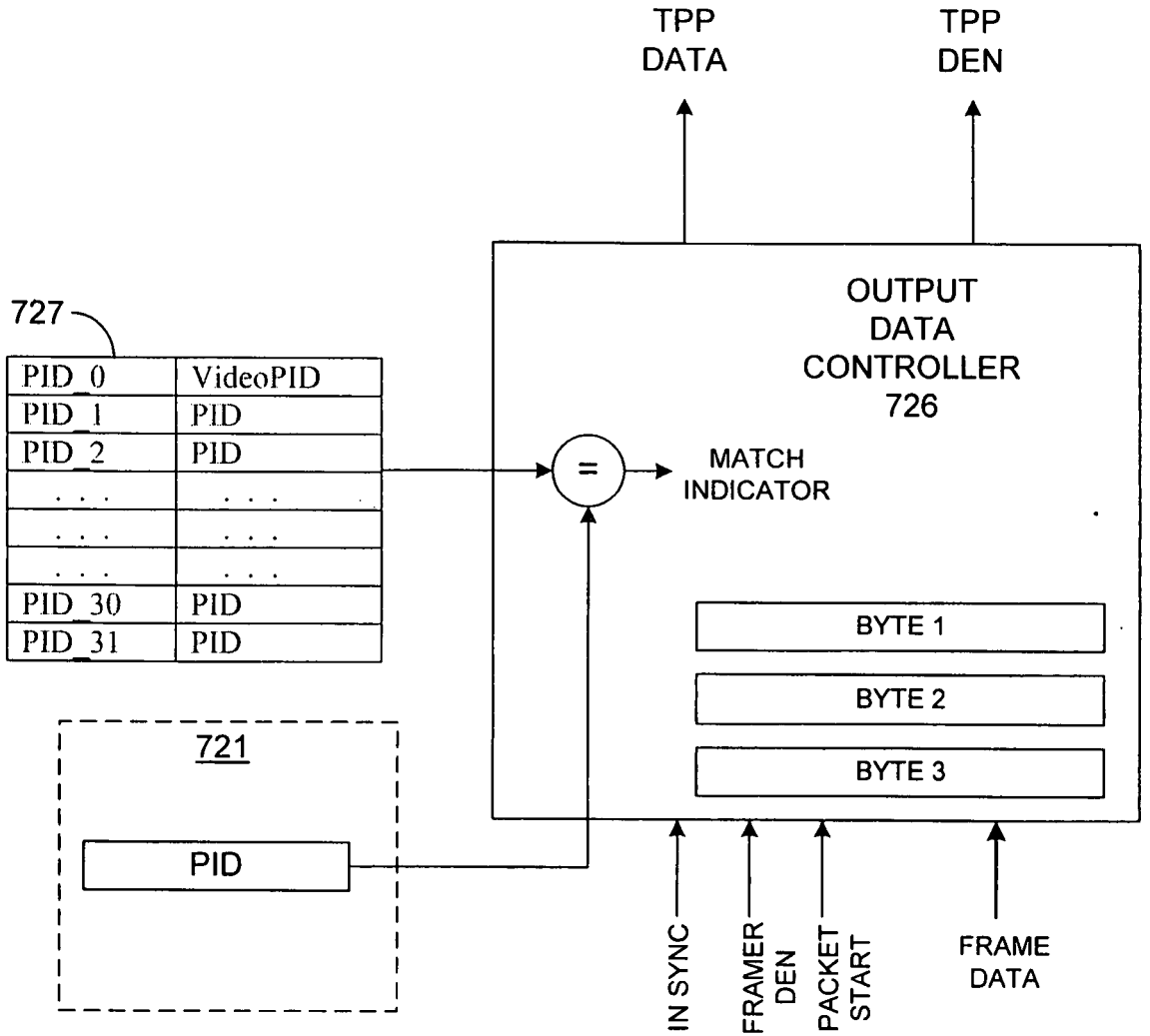


FIGURE 17

Video Control Registers				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
VideoPid	0 -12	[13] 0x1FFF	R/W	Selects a specific PID of the video component stream to filter on. Value of 4095 is reserved one (it means a NULL transport packets).
EnableParsing	13	[1] 0	R/W	If '1' enables parsing from the next transport packet.
StartFromPUSICommand	14	[1] 0	R/W	'0' enables PES parsing immediately. '1' enables PES parsing a transport packet from new PES packet. After that, this bit auto-returns to 0.
ProcessStreamID	15	[1] 0	R/W	If '1' enables parsing on specific stream_id field.
StreamID	16-23	[8] 0xE0	R/W	stream_id of the ES stream to filter on in the PESP.

FIGURE 18

Transport Demultiplexer Registers				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
PID_yz, $0 \le yz \le 30$	0-12	[13] 0x1FFF	R/W	Selects a specific PID of the component stream to filter on. Value of 0x1FFF is reserved (it means a NULL transport packets).
EnableParsing	13	[1] 0	R/W	If set to '1' extraction of defined PID_yz is enabled.
BufferIndex	14-17	[4] 0	R/W	Specifies 1 of 16 destination buffers in the sys. mem.

FIGURE 19

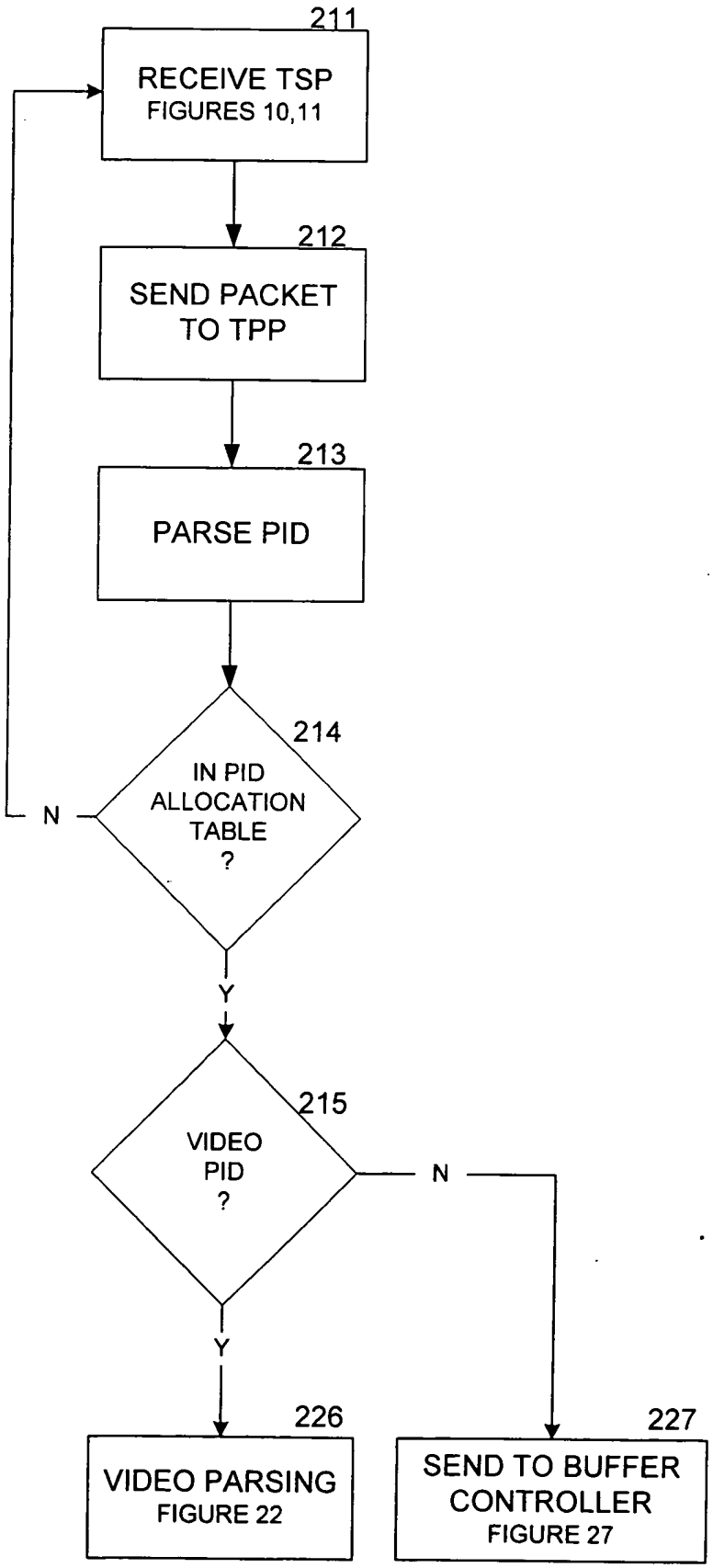

211
RECEIVE TSP
FIGURES 10,11
212
SEND PACKET
TO TPP
213
PARSE PID
214
IN PID
ALLOCATION
TABLE
?
N
Y
215
VIDEO
PID
?
N
Y
226
VIDEO PARSING
FIGURE 22
227
SEND TO BUFFER
CONTROLLER
FIGURE 27

FIGURE 20

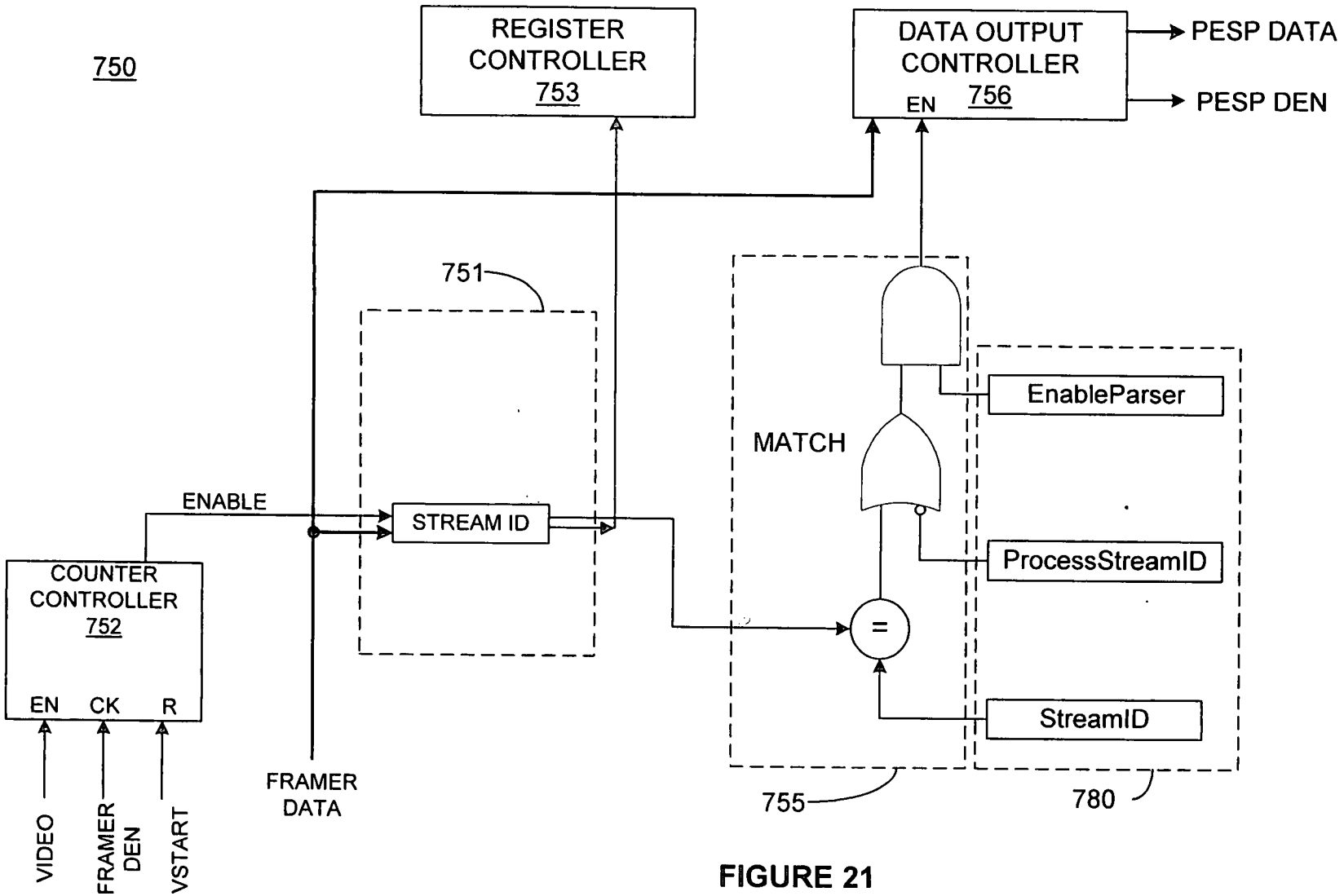


FIGURE 21

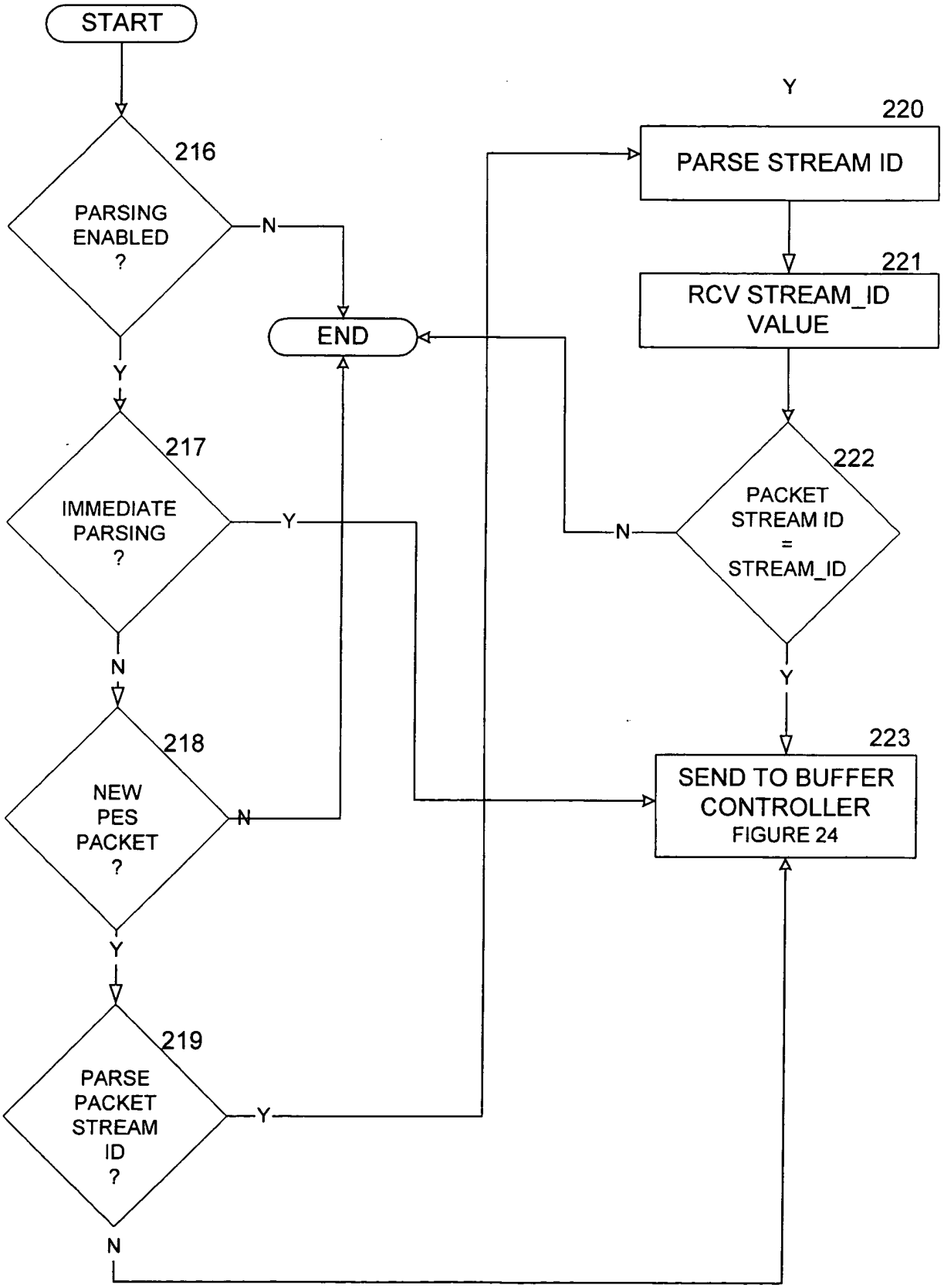

START
216
PARSING ENABLED ?
N
Y
217
IMMEDIATE PARSING ?
Y
N
218
NEW PES PACKET ?
N
Y
219
PARSE PACKET STREAM ID ?
Y
N
END
Y
220
PARSE STREAM ID
221
RCV STREAM_ID VALUE
222
PACKET STREAM ID = STREAM_ID
N
Y
223
SEND TO BUFFER CONTROLLER
FIGURE 24

FIGURE 22

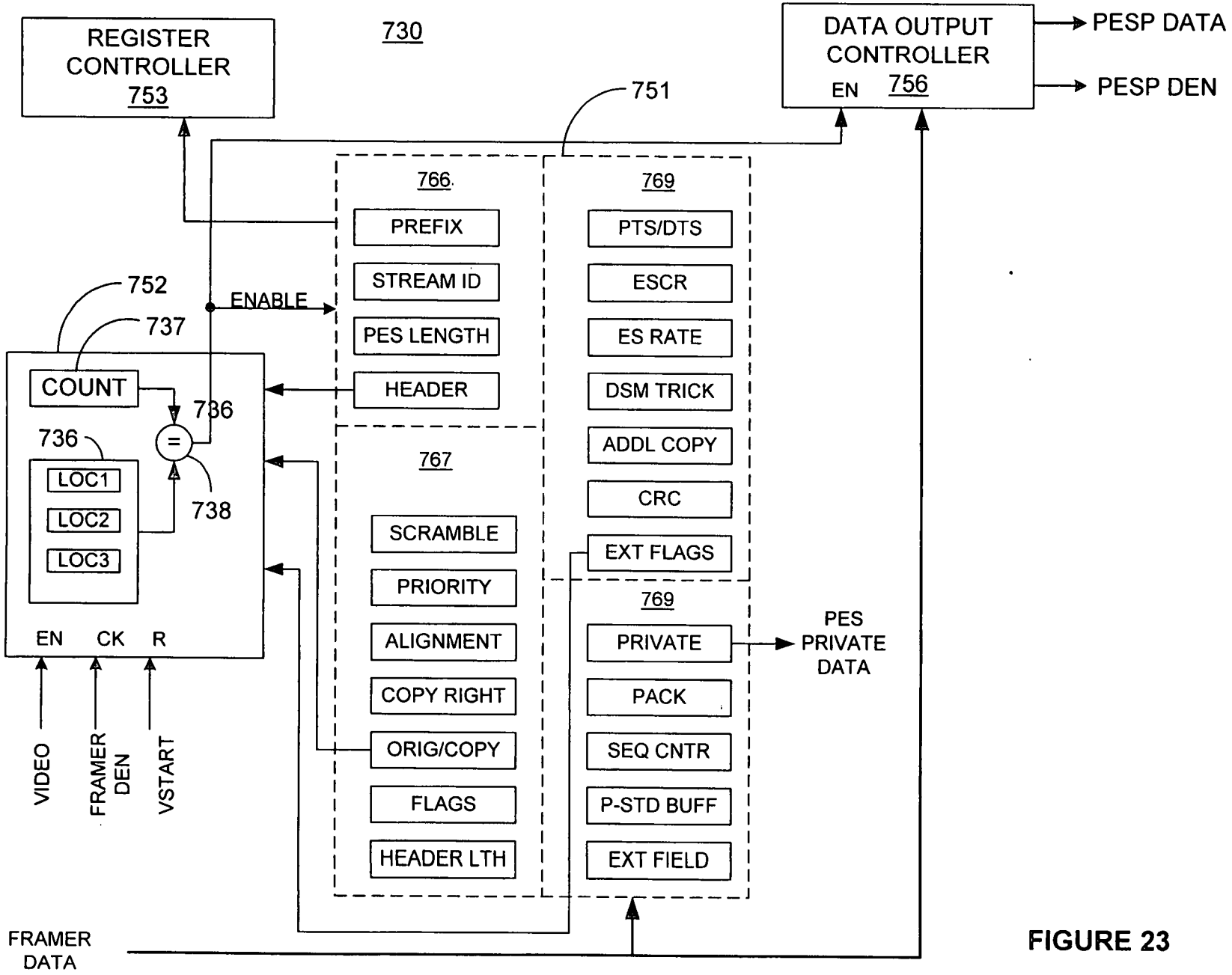

REGISTER CONTROLLER 753
730
DATA OUTPUT CONTROLLER
EN 756
PESP DATA
PESP DEN
751
766
769
PREFIX
STREAM ID
PES LENGTH
HEADER
PTS/DTS
ESCR
ES RATE
DSM TRICK
ADDL COPY
CRC
EXT FLAGS
752
737
ENABLE
COUNT
736
=
736
LOC1
LOC2
LOC3
738
767
SCRAMBLE
PRIORITY
ALIGNMENT
COPY RIGHT
ORIG/COPY
FLAGS
HEADER LTH
769
PRIVATE
PACK
SEQ CNTR
P-STD BUFF
EXT FIELD
PES PRIVATE DATA
EN
CK
R
VIDEO
FRAMER DEN
VSTART
FRAMER DATA

FIGURE 23

Transport Demultiplexer Global Status Register					
Field Name	**Bits**	**Len**	**Default**	**Type**	**Description**
VideoPESHeaderAvailable	12	[1]	0	R/W	This bit is set to '1' when the new PES header of the video stream is received. **WR_ACC_CLEAR.**
VideoPESHeaderError	13	[1]	0	R/W	This bit is set to '1' after an error in the PES header is found. **WR_ACC_CLEAR.**
VideoPESDataAlignment	14	[1]	0	R/W	This bit is set to '1' when video PID has AF *data_alignment_flag*, indicating a possible start of I frame. **WR_ACC_CLEAR.**
VideoPESDSMTrickMode	15	[1]	0	R/W	Indicates that DSM data is found and extracted. **WR_ACC_CLEAR.**
VideoPESPrivateData	16	[1]	0	R/W	This bit is set to '1' when video PID has 16 bytes of private data in the PES header. **WR_ACC_CLEAR.**
VideoPESCRCError	17	[1]	0	R/W	This bit is set to '1' if the video CRC of the PESP parser found a CRC mismatch. **WR_ACC_CLEAR.**

Figure 24

Transport Demultiplexer Interrupt Mask Register				
Field Name	**Bits**	**Len**	**Default**	**Type**	**Description**
EventInterruptMask	0-18	[19]	0	R/W	If set to '1' enables local sources Bit 12 – VideoPESHeaderAvailable Bit 13 – VideoPESHeaderError Bit 14 – VideoPESDataAlignment Bit 15 – VideoPESDSMTrickMode Bit 16 – VideoPESPrivateData Bit 17 – VideoPESCRCError Bit 18 – VideoPTSReceived Bit 19 – VideoESCRReceived

Figure 25

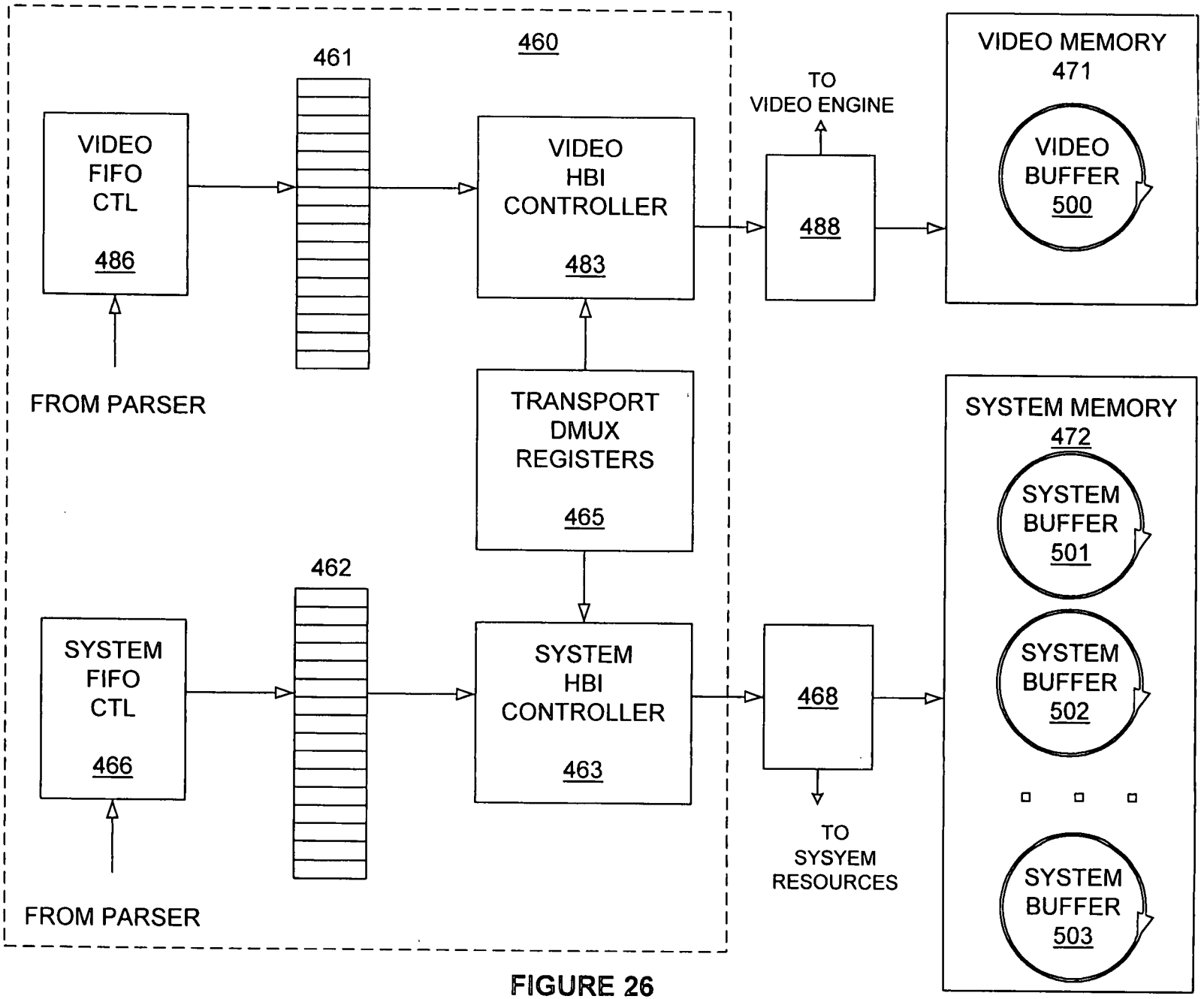

460
461
VIDEO FIFO CTL
486
FROM PARSER
VIDEO HBI CONTROLLER
483
TO VIDEO ENGINE
488
VIDEO MEMORY
471
VIDEO BUFFER
500
TRANSPORT DMUX REGISTERS
465
462
SYSTEM FIFO CTL
466
FROM PARSER
SYSTEM HBI CONTROLLER
463
468
TO SYSYEM RESOURCES
SYSTEM MEMORY
472
SYSTEM BUFFER
501
SYSTEM BUFFER
502
SYSTEM BUFFER
503

FIGURE 26

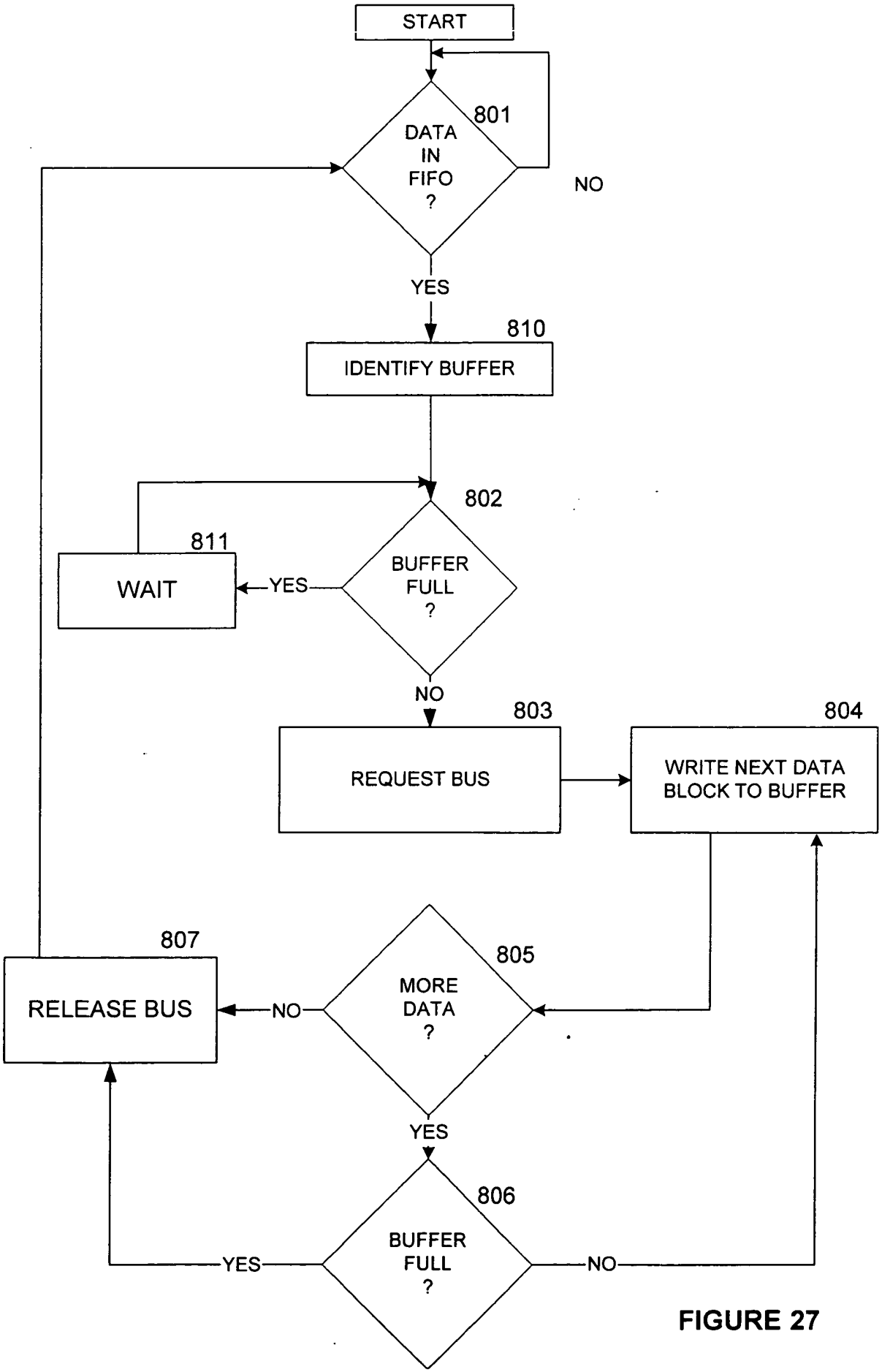

START
801
DATA IN FIFO ?
NO
YES
810
IDENTIFY BUFFER
802
BUFFER FULL ?
YES
811
WAIT
NO
803
REQUEST BUS
804
WRITE NEXT DATA BLOCK TO BUFFER
805
MORE DATA ?
NO
807
RELEASE BUS
YES
806
BUFFER FULL ?
YES
NO

FIGURE 27

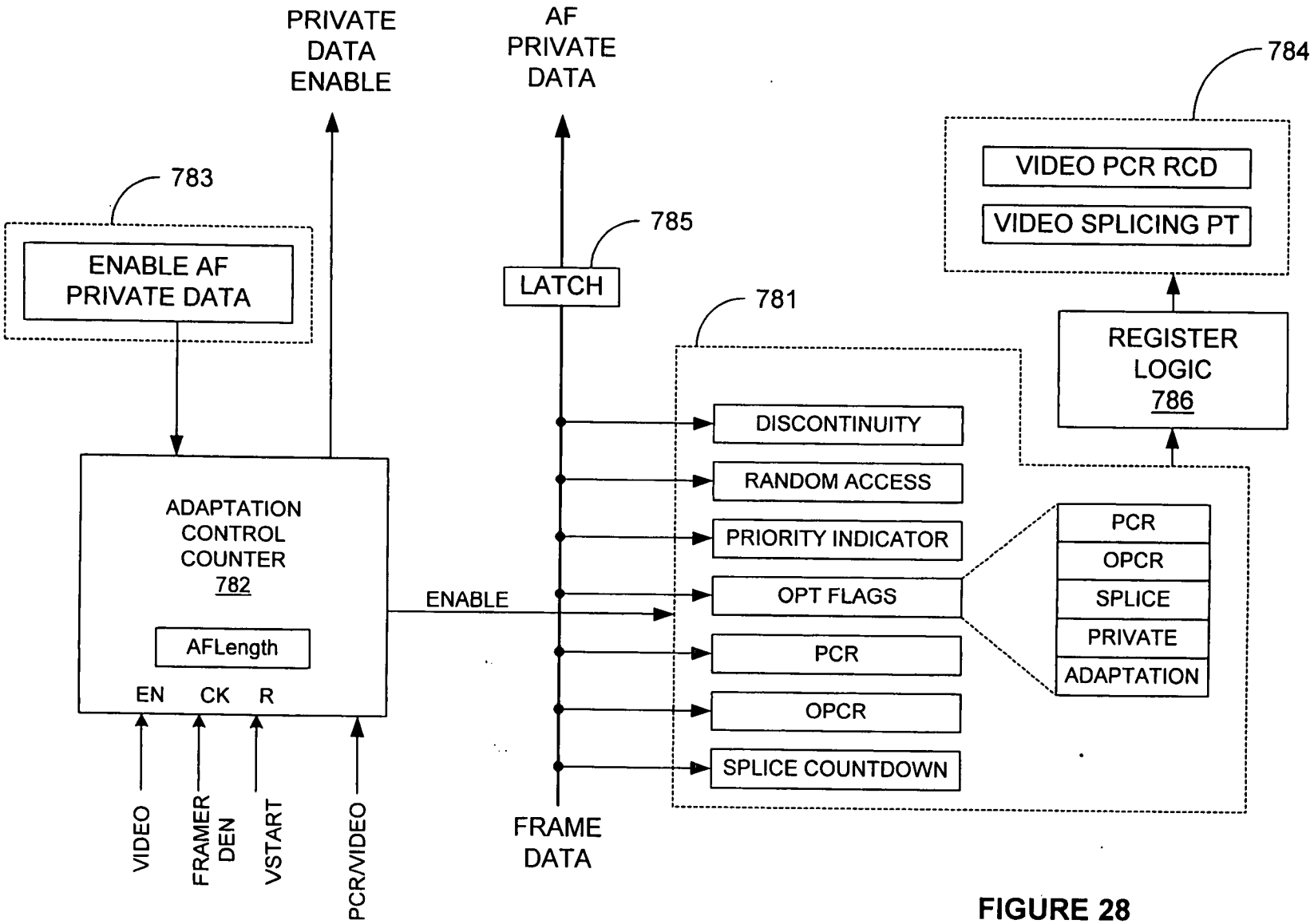

PRIVATE DATA ENABLE
AF PRIVATE DATA
784
VIDEO PCR RCD
VIDEO SPLICING PT
783
ENABLE AF PRIVATE DATA
785
LATCH
781
REGISTER LOGIC 786
DISCONTINUITY
RANDOM ACCESS
PRIORITY INDICATOR
OPT FLAGS
PCR
OPCR
SPLICE
PRIVATE
ADAPTATION
ADAPTATION CONTROL COUNTER 782
AFLength
EN CK R
ENABLE
PCR
OPCR
SPLICE COUNTDOWN
VIDEO
FRAMER DEN
VSTART
PCR/VIDEO
FRAME DATA

FIGURE 28

Transport Demultiplexer Global Status Register				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
VideoAFPcrReceived	[1]	0	R/W	This bit is set to '1' after arrival and extraction of PCR sample in the adaptation field. **WR_ACC_CLEAR.**
VideoAFPcrDiscontinuity	[1]	0	R/W	This bit is set to '1' when a *discontinuity_indicator* in The adaptation field of the PCR PID is asserted. **WR_ACC_CLEAR.**
VideoAFDiscontinuityFlag	[1]	0	R/W	This bit is set to '1' after a *discontinuity_indicator_flag* has been asserted in the AF of video TP, indicating a discontinuity on continuity_counter. **WR_ACC_CLEAR.**
VideoAFRandomAccess	[1]	0	R/W	This bit is set to '1' when video PID *has random_ access_flag* asserted in the AF, indicating a start of the elementary stream. **WR_ACC_CLEAR.**
VideoAFSplicingFlag	[1]	0	R/W	This bit is set to '1' when video PID has *splicing_ point_flag* asserted in the AF, indicating approaching of the splicing point. **WR_ACC_CLEAR.**
VideoAFSplicingPoint	[1]	0	R/W	This bit is set to '1' when video PID has *splicing_ point_flag* asserted in the AF, after splicing point occurred (splice_countdown =0). **WR_ACC_CLEAR.**
VideoAFPrivateData	[1]	0	R/W	This bit is set to '1' when video has AF private data. **WR_ACC_CLEAR.**
AFSpliceCountdown	[8]	0x00	R/W	Current splice countdown value from adaptation field of A/V packets. Modified on the fly by AF content

Figure 29

Transport Demultiplexer Interrupt Mask Register				
Field Name	**Bits**	**Len Default**	**Type**	**Description**
EventInterruptMask	0-18	[19] 0	R/W	If set to '1' enables local sources Bit 5 – VideoAFPcrReceived Bit 6 – VideoAFPcrDiscontinuity Bit 7 – VideoAFDiscontinuityFlag Bit 8 – VideoAFRandomAccessFlag Bit 9 – VideoAFSplicingFlag Bit 10 – VideoAFSplicingPoint Bit 11 – VideoAFPrivateData

Figure 30

Transport Demultiplexer Global Control Register					
Field Name	**Bits**	**Len**	**Default**	**Type**	**Description**
EnableAFPrivateData	[1]		0	R/W	If '1' enables parsing and routing of AF private data
AFPrivateDataBufferIndex	[4]		0	R/W	Specifies 1 of 15 destination buffers in the system memory
PCRIndex	[1]		0	R/W	
EnableAutoSplicing	[1]		0	R/W	

Figure 31

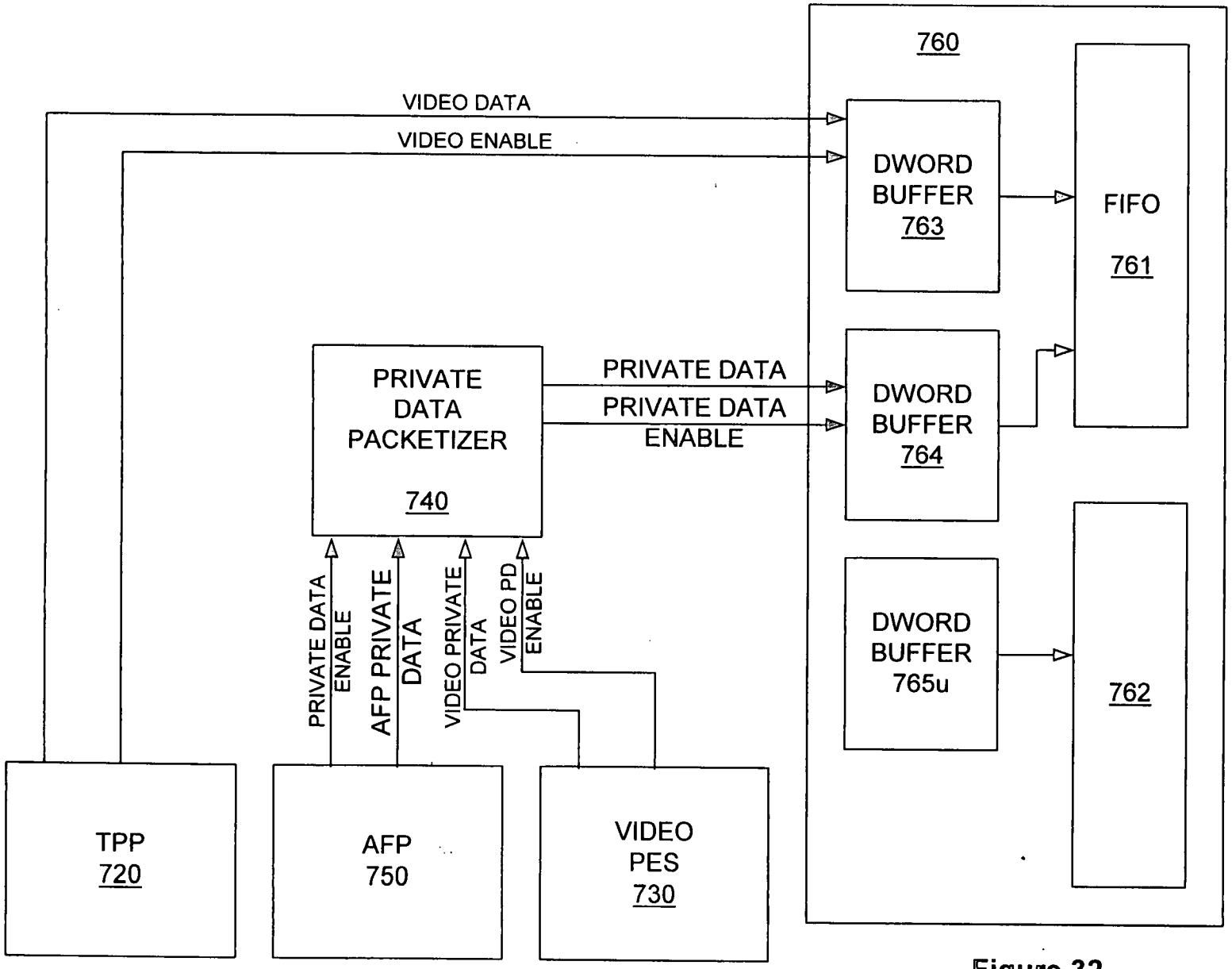


Figure 32

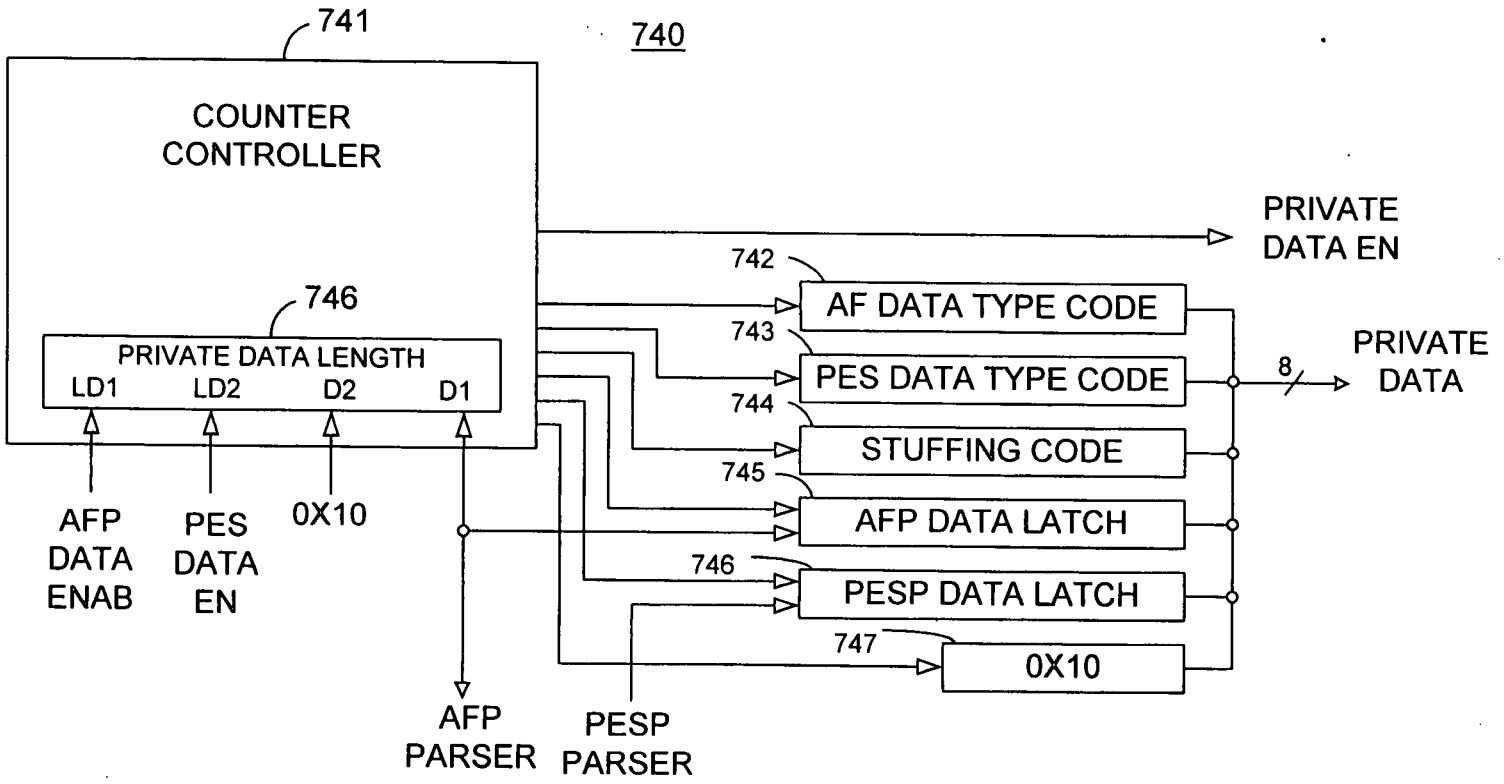

741
740
COUNTER CONTROLLER
746
PRIVATE DATA LENGTH
LD1
LD2
D2
D1
AFP DATA ENAB
PES DATA EN
0X10
AFP PARSER
PESP PARSER
PRIVATE DATA EN
742
AF DATA TYPE CODE
743
PES DATA TYPE CODE
744
STUFFING CODE
745
AFP DATA LATCH
746
PESP DATA LATCH
747
0X10
8
PRIVATE DATA

Figure 33

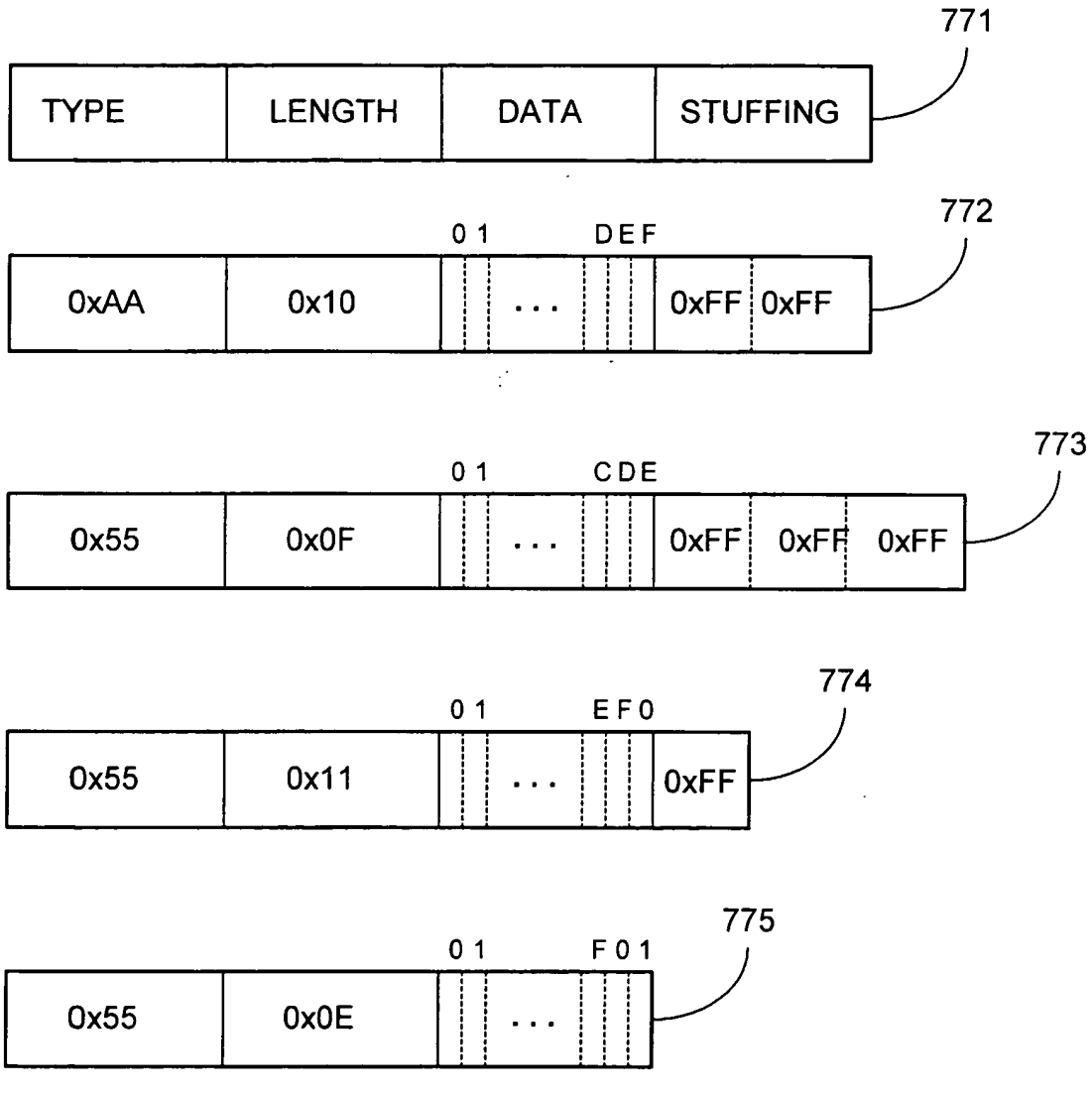

771
TYPE
LENGTH
DATA
STUFFING
772
0 1
D E F
0xAA
0x10
. . .
0xFF
0xFF
773
0 1
C D E
0x55
0x0F
. . .
0xFF
0xFF
0xFF
774
0 1
E F 0
0x55
0x11
. . .
0xFF
775
0 1
F 0 1
0x55
0x0E
. . .

Figure 34

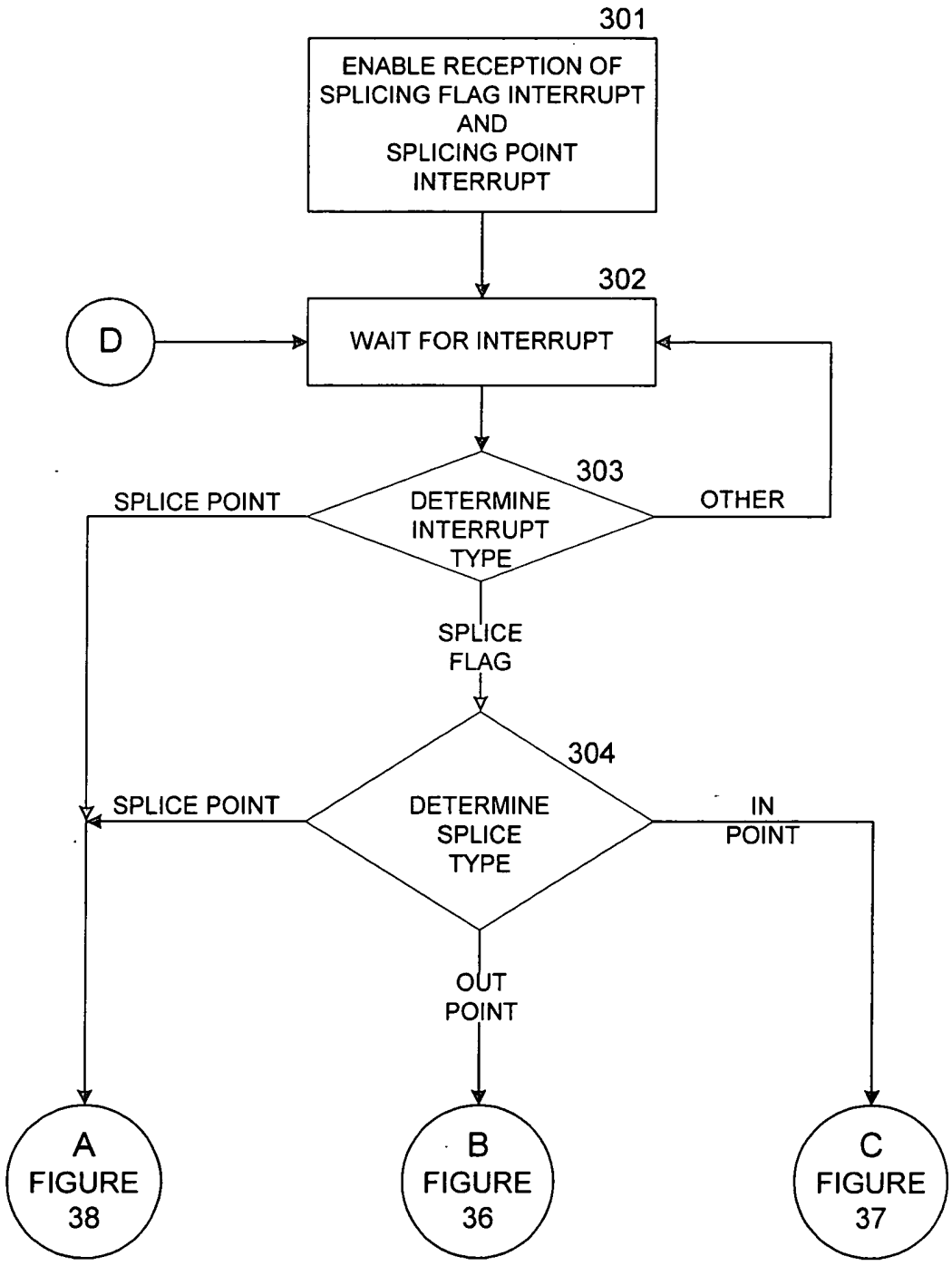

301
ENABLE RECEPTION OF SPLICING FLAG INTERRUPT AND SPLICING POINT INTERRUPT
302
D
WAIT FOR INTERRUPT
303
SPLICE POINT
DETERMINE INTERRUPT TYPE
OTHER
SPLICE FLAG
304
SPLICE POINT
DETERMINE SPLICE TYPE
IN POINT
OUT POINT
A FIGURE 38
B FIGURE 36
C FIGURE 37

FIGURE 35

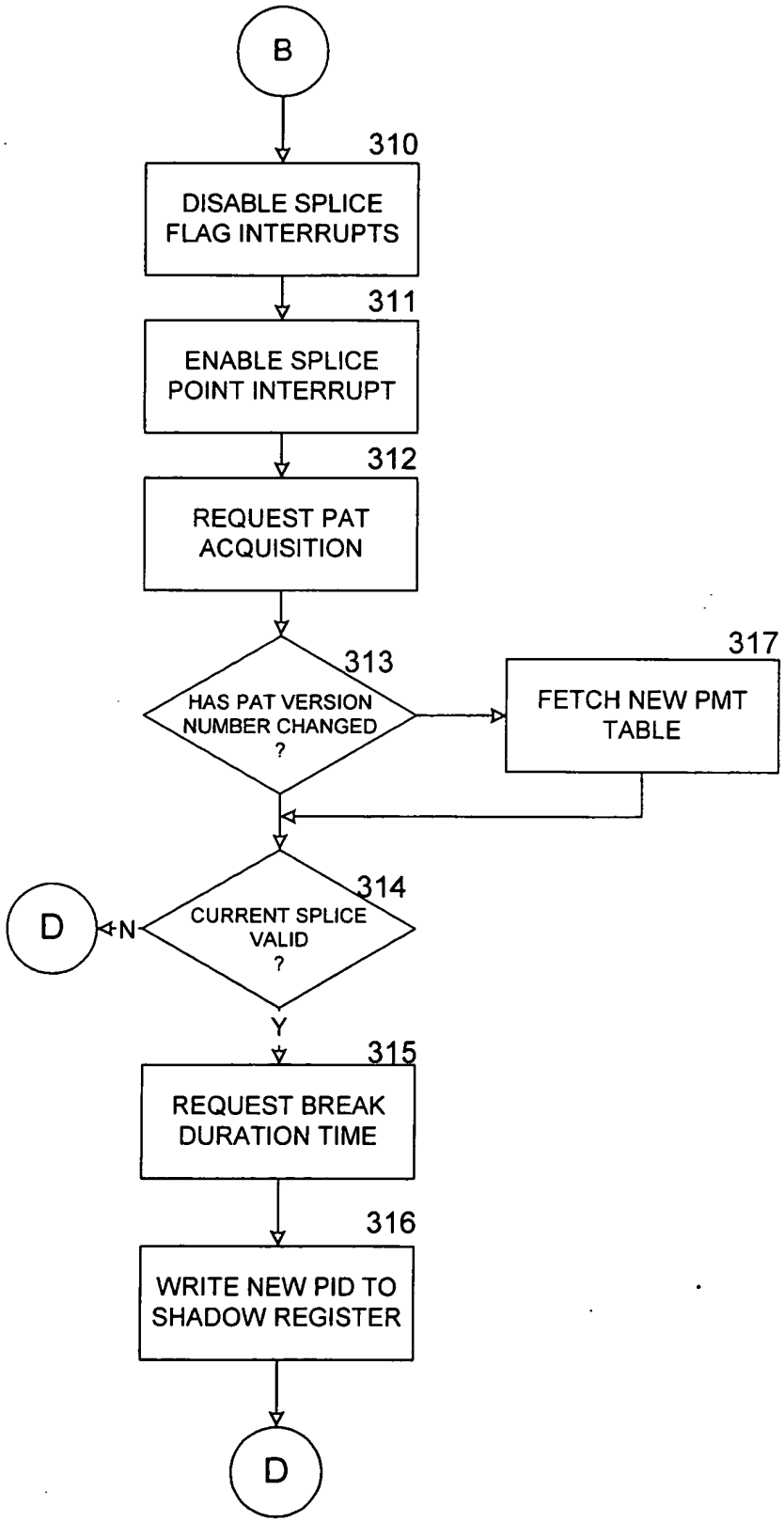

B
310
DISABLE SPLICE FLAG INTERRUPTS
311
ENABLE SPLICE POINT INTERRUPT
312
REQUEST PAT ACQUISITION
313
HAS PAT VERSION NUMBER CHANGED ?
317
FETCH NEW PMT TABLE
314
CURRENT SPLICE VALID ?
N
D
Y
315
REQUEST BREAK DURATION TIME
316
WRITE NEW PID TO SHADOW REGISTER
D

FIGURE 36

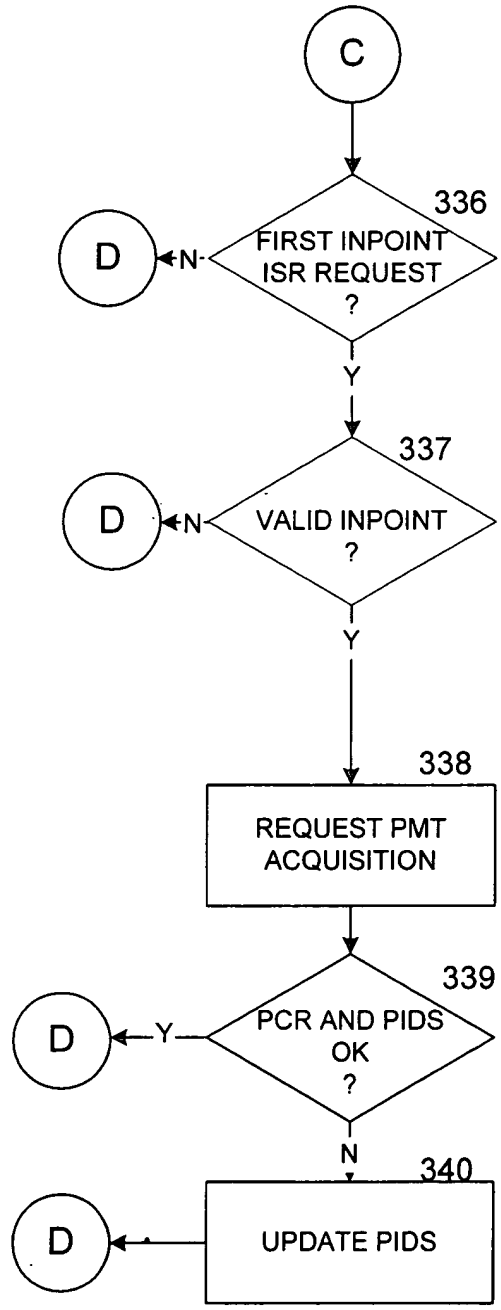

C
336
FIRST INPOINT ISR REQUEST ?
D
N
Y
337
VALID INPOINT ?
D
N
Y
338
REQUEST PMT ACQUISITION
339
PCR AND PIDS OK ?
D
Y
N
340
UPDATE PIDS
D

FIGURE 37

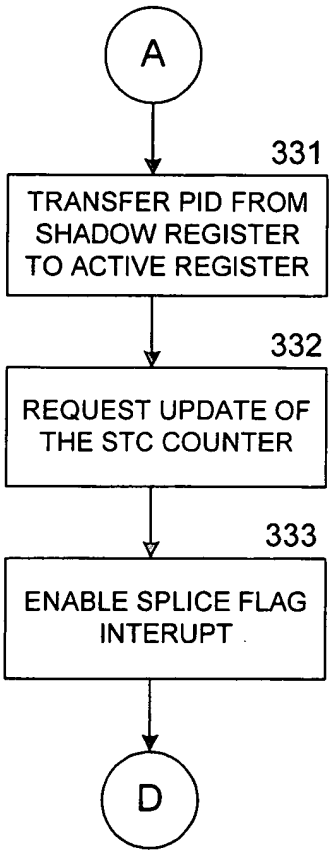

A
331
TRANSFER PID FROM SHADOW REGISTER TO ACTIVE REGISTER
332
REQUEST UPDATE OF THE STC COUNTER
333
ENABLE SPLICE FLAG INTERUPT
D

FIGURE 38

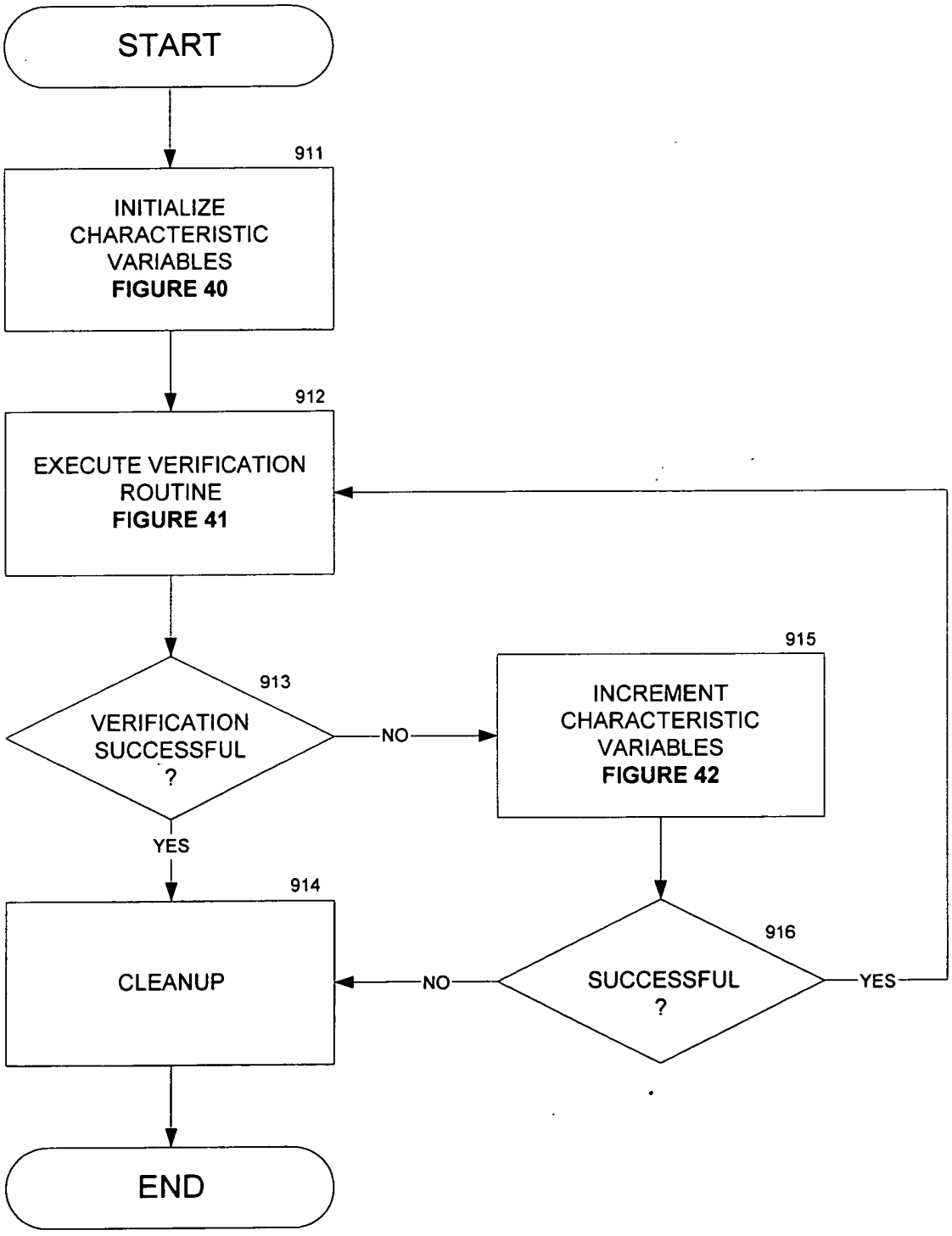

START
911
INITIALIZE CHARACTERISTIC VARIABLES
FIGURE 40
912
EXECUTE VERIFICATION ROUTINE
FIGURE 41
913
VERIFICATION SUCCESSFUL ?
NO
915
INCREMENT CHARACTERISTIC VARIABLES
FIGURE 42
YES
914
CLEANUP
NO
916
SUCCESSFUL ?
YES
END

FIGURE 39

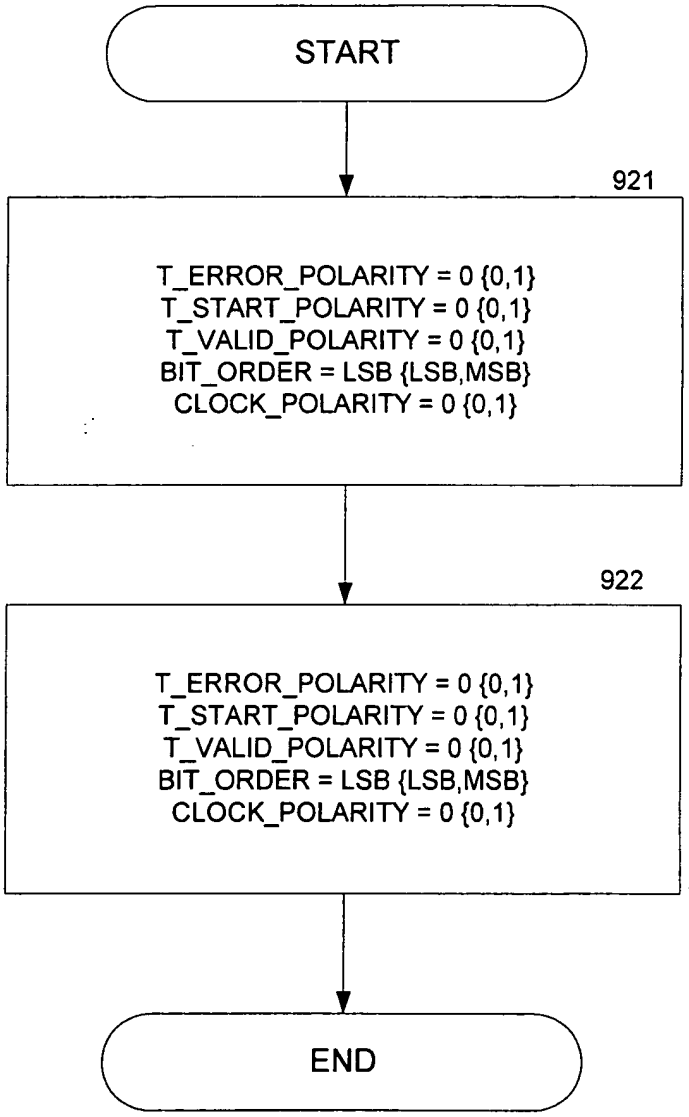

START
921
T_ERROR_POLARITY = 0 {0,1}
T_START_POLARITY = 0 {0,1}
T_VALID_POLARITY = 0 {0,1}
BIT_ORDER = LSB {LSB,MSB}
CLOCK_POLARITY = 0 {0,1}
922
T_ERROR_POLARITY = 0 {0,1}
T_START_POLARITY = 0 {0,1}
T_VALID_POLARITY = 0 {0,1}
BIT_ORDER = LSB {LSB,MSB}
CLOCK_POLARITY = 0 {0,1}
END

FIGURE 40

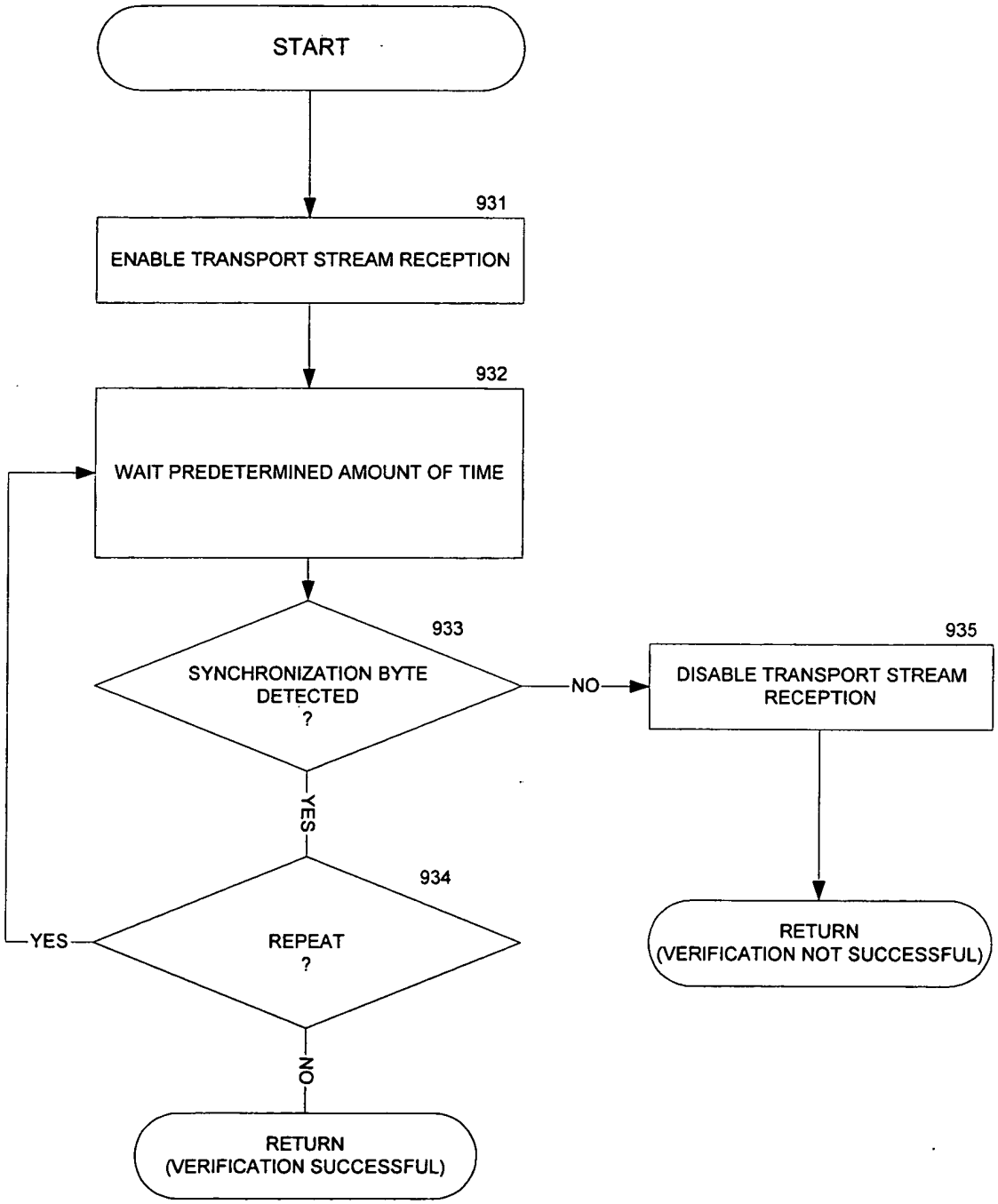

START
931
ENABLE TRANSPORT STREAM RECEPTION
932
WAIT PREDETERMINED AMOUNT OF TIME
933
SYNCHRONIZATION BYTE DETECTED ?
NO
935
DISABLE TRANSPORT STREAM RECEPTION
YES
934
REPEAT ?
YES
RETURN (VERIFICATION NOT SUCCESSFUL)
NO
RETURN (VERIFICATION SUCCESSFUL)

FIGURE 41

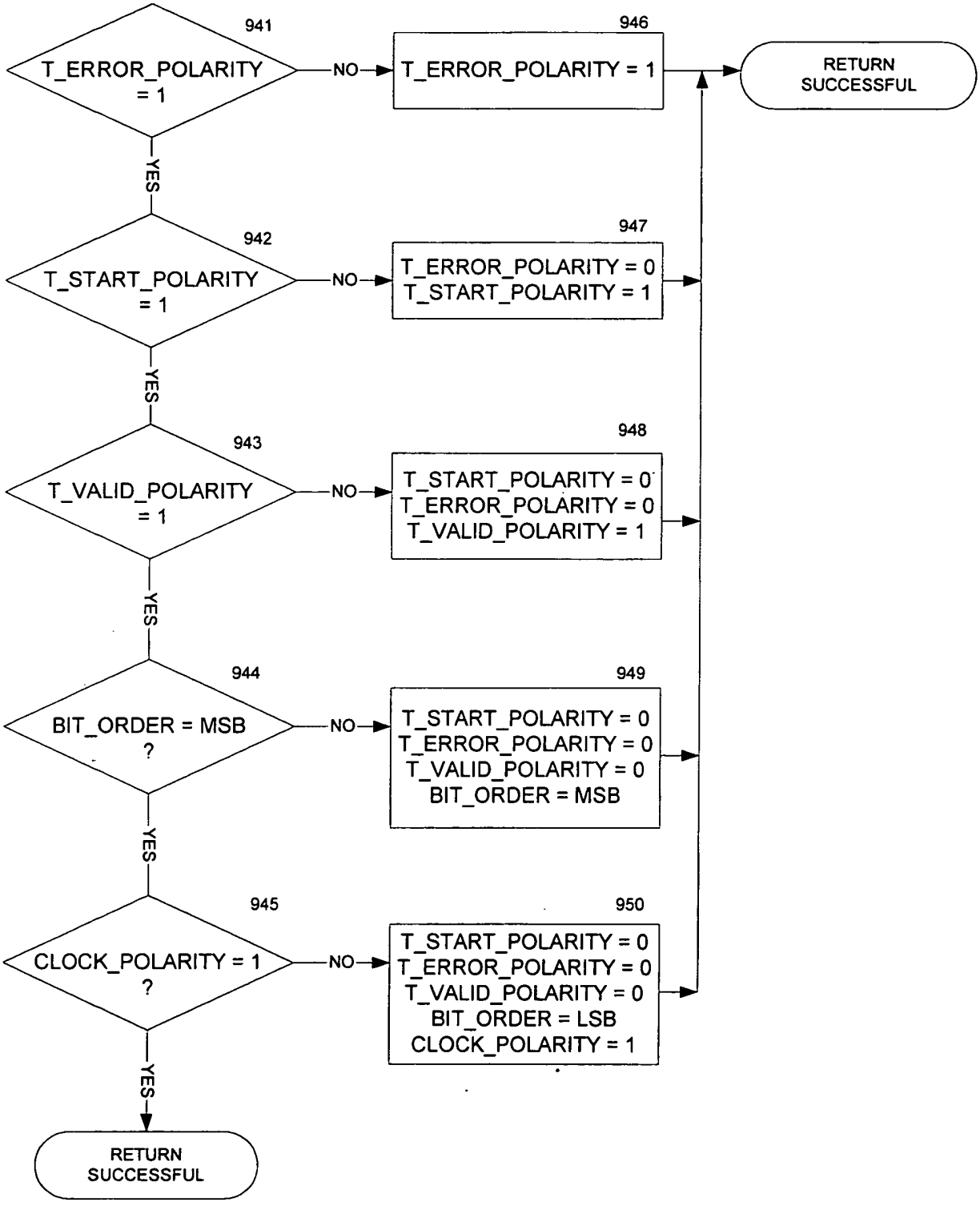

941
T_ERROR_POLARITY = 1
NO
946
T_ERROR_POLARITY = 1
RETURN SUCCESSFUL
YES
942
T_START_POLARITY = 1
NO
947
T_ERROR_POLARITY = 0
T_START_POLARITY = 1
YES
943
T_VALID_POLARITY = 1
NO
948
T_START_POLARITY = 0
T_ERROR_POLARITY = 0
T_VALID_POLARITY = 1
YES
944
BIT_ORDER = MSB ?
NO
949
T_START_POLARITY = 0
T_ERROR_POLARITY = 0
T_VALID_POLARITY = 0
BIT_ORDER = MSB
YES
945
CLOCK_POLARITY = 1 ?
NO
950
T_START_POLARITY = 0
T_ERROR_POLARITY = 0
T_VALID_POLARITY = 0
BIT_ORDER = LSB
CLOCK_POLARITY = 1
YES
RETURN SUCCESSFUL

FIGURE 42

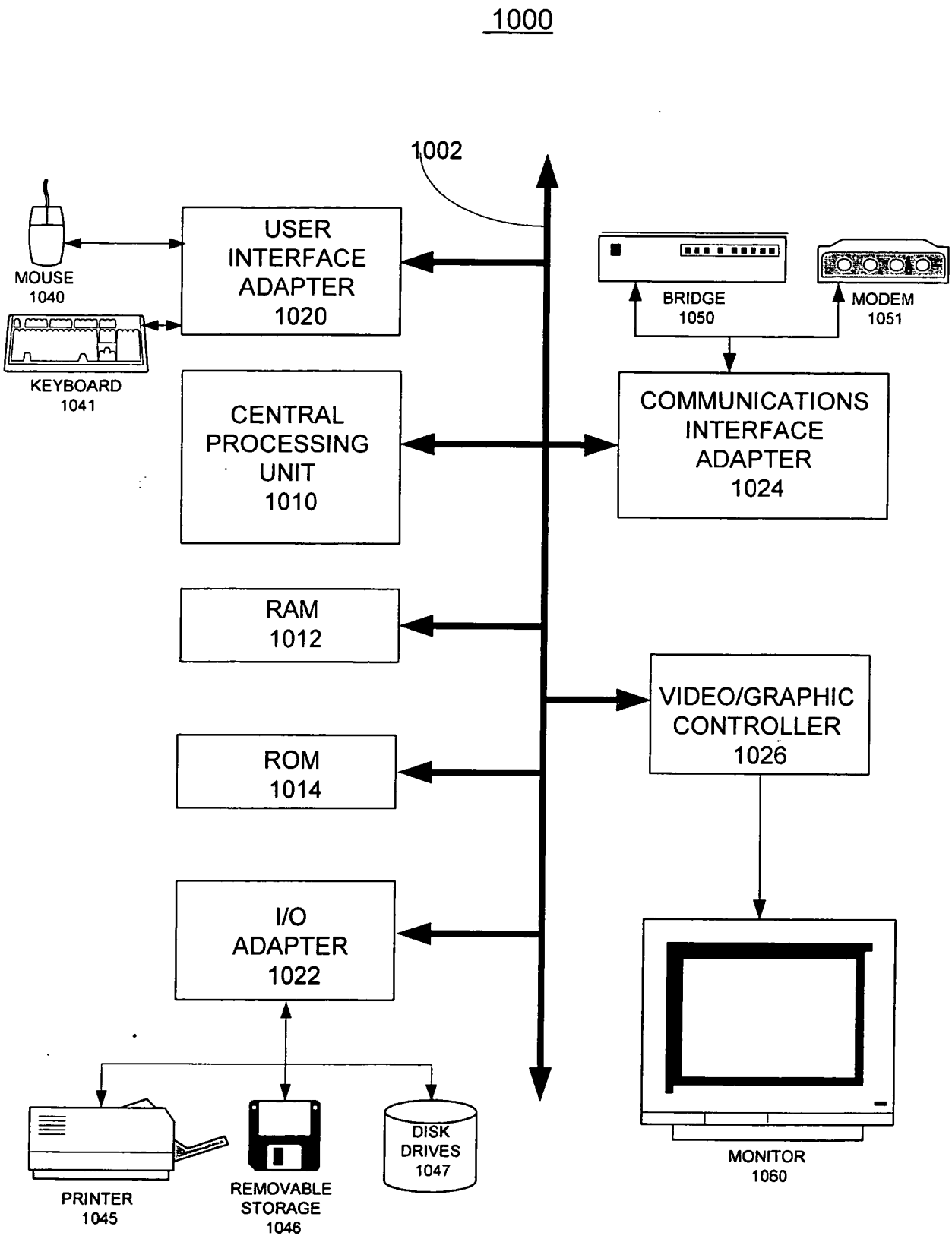

1000
1002
USER INTERFACE ADAPTER 1020
MOUSE 1040
KEYBOARD 1041
BRIDGE 1050
MODEM 1051
CENTRAL PROCESSING UNIT 1010
COMMUNICATIONS INTERFACE ADAPTER 1024
RAM 1012
VIDEO/GRAPHIC CONTROLLER 1026
ROM 1014
I/O ADAPTER 1022
DISK DRIVES 1047
MONITOR 1060
PRINTER 1045
REMOVABLE STORAGE 1046

FIGURE 43